THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Millimeter-Wave Active Array Antennas Integrating Power Amplifier MMICs through Contactless Interconnects

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Abstract

Next-generation mobile wireless technologies demand higher data capacity than the modern sub-6 GHz technologies can provide. With abundantly available bandwidth, millimeter waves (e.g., K_a/K bands) can offer data rates of around 10 Gbit/s; however, this shift to higher frequency bands also leads to at least 20 dB more free-space path loss. Active integrated antennas have drawn much attention to compensate for this increased power loss with high-power, energy-efficient, highly integrated array transmitters.

Traditionally, amplifiers and antennas are designed separately and interconnected with 50 Ohm intermediate impedance matching networks. The design process typically de-emphasizes the correlation between antenna mutual coupling effects and amplifier nonlinearity, rendering high power consumption and poor linearity. This research aims to overcome the technical challenges of millimeter-wave active integrated array antennas on delivering high power (15–25 dBm) and high energy efficiency ($\geq$25%) with above 10% bandwidth.

A co-design methodology was proposed to maximize the output power, power efficiency, bandwidth, and linearity with defined optimal interface impedances. Contrary to conventional approaches, this methodology accounts for the correlation between mutual coupling effects and nonlinearity. A metallic cavity-backed bowtie slot antenna, with sufficient degrees of freedom in synthesizing a non 50 Ohm complex-valued optimal impedance, was adopted for high radiation efficiency and enhanced bandwidth. To overcome interconnection's bandwidth and power loss limitations, an on-chip E-plane probe contactless transition between the antenna and amplifier was proposed. An array of such antennas becomes connected bowtie slots, allowing for wideband and wide-scan array performance. An infinite array active integrated unit cell approach was introduced for large-scale (aperture area $\approx 100\,\lambda^2$) active array designs.

The proposed co-design flow is applied in designing a K_a-band wideband, wide scan angle ($\pm 55°/\pm 40°$) active array antenna, consisting of the connected bowtie slot radiator fed through the on-chip probe integrated onto the output of a class AB GaAs *p*HEMT MMIC PA. The infinite array performance of such elements is experimentally verified, presenting a 11.3% bandwidth with a peak 40% power efficiency, 28 dBm EIRP, and 22 dBm saturated power.

Keywords: Integrated active antenna, power amplifier, MMIC, contactless transition.

List of Publications

This thesis is based on the following publications:

[A] **W.-C. Liao**, R. Maaskant, T. Emanuelsson, M. Johansson, A. Höök, J. Wettergren, M. Dieudonne, M. V. Ivashina, "A Ka-Band Active Integrated Antenna for 5G Applications: Initial Design Flow". *Published in IEEE 2nd URSI AT-RASC*, May 2018.

[B] **W.-C. Liao**, R. Maaskant, T. Emanuelsson, V. Vassilev, O. A. Iupikov, M. V. Ivashina, "A Directly Matched PA-Integrated *K*-band Antenna for Efficient mm-Wave High-Power Generation". *Published in IEEE Antennas and Wireless Propagation Letters*, Nov. 2019.

[C] **W.-C. Liao**, R. Maaskant, T. Emanuelsson, A. R. Vilenskiy, M. V. Ivashina, "Antenna Mutual Coupling Effects in Highly Integrated Transmitter Arrays". *Published in Proceeding 2020 14th European Conference on Antennas and Propagation (EuCAP)*, March 2020.

[D] **W.-C. Liao**, T. Emanuelsson, R. Maaskant, A. R. Vilenskiy, T. Eriksson, M. V. Ivashina, "Power Efficiency and Linearity of Highly Integrated Transmitting Array Antennas". *Published in Proceeding 2021 15th European Conference on Antennas and Propagation (EuCAP)*, March 2021.

[E] A. R. Vilenskiy, **W.-C. Liao**, R. Maaskant, V. Vassilev, O. A. Iupikov, T. Emanuelsson, M. V. Ivashina, "Co-Design and Validation Approach for Beam-Steerable Phased Arrays of Active Antenna Elements with Integrated Power Amplifiers". *Published in IEEE Transactions on Antennas and Propagation*, Nov. 2021.

[F] **W.-C. Liao**, A. R. Vilenskiy, R. Maaskant, T. Emanuelsson, V. Vassilev, M. V. Ivashina, "mmWave Bowtie Connected-Slot Array Element Integrating Power Amplifier MMIC via On-Chip Probe to Enhance Efficiency and Bandwidth". *In preparation for submitting to IEEE Transactions on Antennas and Propagation*.

Other publications by the author, not included in this thesis, are:

[G] R. Maaskant, O. A. Iupikov, C. A. H. M. van Puijenbroek, **W.-C. Liao**, M. Matters-Kammerer, M. V. Ivashina, "Deep Integration Antenna Array: Design Philosophy and Principles". *Proc. 13th European Conference on Antennas and Propagation (EuCAP)*, Krakow, Poland, Apr. 2019.

[H] J. Fan, K. Zhu, J. Yang, H. Yuan, P. Jiang, Y. Yan, **W.-C. Liao**, H. Cao, J. Ma, B. Li, "Design of Novel Flat Bend Crossed Dipole for Wideband Phased Array Feed Applications". *Proc. 2019 International Symposium on Antennas and Propagation (ISAP)* Xian, China, Oct. 2019.

[I] I. Aziz, **W.-C. Liao**, H. Aliakbari, "Compact and Low Cost Linear Antenna Array for Millimeter Wave Automotive Radar Applications". *Proc. 14th European Conference on Antennas and Propagation (EuCAP)*, Copenhagen, Denmark, Apr. 2020.

[J] J. Fan, J. Yang, Y. Yan, **W.-C. Liao**, D. Zhan, "Investigation of Ultra-wideband Bowtie Antennas for Phased Array Feed Application". *International Journal of RF and Microwave Computer-Aided Engineering*, 2020.

[K] **W.-C. Liao**, R. Maaskant, A. V. Vilenskiy, T. Emanuelsson, M. V. Ivashina, "Contactless Chip-to-Waveguide Transition of GaAs MMIC for Active Array Antennas". *IEEE Microwave and Wireless Components Letters* (in preparation).

Preface

This thesis is in partial fulfillment for the degree of Doctor of Philosophy at Chalmers University of Technology, Gothenburg, Sweden.

The work resulting in this thesis was carried out between May 2017 and November 2021 in the Antenna Systems group, Department of Electrical Engineering, Chalmers. Professor Marianna Ivashina is the main supervisor and the examiner. In addition, Assistant Professor Rob Maaskant and Adjunct Professor Thomas Emanuelsson are the co-supervisors.

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Wan-Chun
Göteborg, November 2021

Acronyms

5G	The Fifth Generation of Mobile Wireless Technologies
ADS	Advanced Design System
AIA	Active Integrated Antenna
AIAA	Active Integrated Array Antenna
AIAiP	Active Integrated Antenna-in-Package
AiP	Antenna-in-Package
AIUC	Active Integrated Unit Cell
AMC	Artificial Magnetic Conductor
AoC	Antenna-on-Chip
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DRC	Design Rule Checking
DUT	Device Under Test
EIRP	Equivalent Isotropic Radiated Power
EM	Electromagnetic
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSG	Ground-signal-ground
HBT	Heterojunction Bipolar Transistor

HEMT	High Electron Mobility Transistor
IC	Integrated Circuit
IMD	Intermodulation Distortion
IMN	Impedance Matching Network
MC	Mutual Coupling
MMIC	Monolithic Microwave Integrated Circuit
MIMO	Multiple-Input, Multiple-Output
MU-MIMO	Multi-User, Multiple-Input, Multiple-Output
mmWave	Millimeter-Wave
NR	New Radio
OTA	Over-The-Air
PA	Power Amplifier
PAE	Power-Added Efficiency
PAIAA	Power Amplifier-Integrated Active Antenna
PBC	Periodic Boundary Condition
PCB	Printed Circuit Board
***p*HEMT**	Pseudomorphic High Electron Mobility Transistor
RF	Radio Frequency
SiGe	Silicon Germanium
SoC	System-on-Chip
TOI	Third-Order Intercept point
WG	Waveguide

CONTENTS

Part I

Introductory Chapters

CHAPTER 1

INTRODUCTION

This chapter introduces the research area of this Ph.D. thesis, *millimeter-wave integrated active array antennas*, and contains a brief overview of design challenges in millimeter-wave wireless communication systems and existing integrated antenna technologies. The scientific contributions and outline of this thesis are summarized thereafter.

1.1 Motivation

The continuously increasing demand in data capacity and throughput for next-generation wireless communication requires a technological evolution to deliver broadband capabilities and advanced wireless connectivity for the primary usage scenarios. This evolution shifts new technological solutions from the traditional sub-6 GHz to the millimeter-wave (mmWave) frequencies [1], [2], where the available bandwidths can be in the order of gigahertz, enabling higher system capacity.

Wireless connectivity of communication systems is constrained by the link budget. It depends on the antenna gain, power gain and losses in the communication system, and the operating frequency. The *Friis Transmission Equation* relates the power received from one antenna when transmitted from another antenna. The receiving antenna is located in the far field ($R > 2D^2/\lambda$) of the transmitting antenna, where D is the largest dimension of either antenna, and λ is the free space wavelength. The ratio of the received to the transmitted power (P_r and P_t) can be expressed by

$$\frac{P_r}{P_t} = \frac{\lambda^2 \eta_t \eta_r D_t(\theta_t, \phi_t) D_r(\theta_r, \phi_r)}{(4\pi R)^2} = \left(\frac{\lambda}{4\pi R}\right)^2 G_t(\theta_t, \phi_t) G_r(\theta_r, \phi_r) \tag{1.1}$$

where η_t, η_r are the radiation efficiency of the transmitting and receiving antennas, D_t, D_r are

their directivity values, and G_t, G_r are their gains in the direction θ_t, ϕ_t and θ_r, ϕ_r[1], respectively [3]. The *free-space path loss (FSPL)* is obtained by $(4\pi R/\lambda)^2$, i.e., reduction in power density of electromagnetic (EM) waves as an EM wave propagates through the free space between the transmitting and receiving antennas. Assuming that the transmitter and the receiver hardware remain the same, increasing the operating frequency means increased FSPL. The most intuitive solutions to improve the transmitter in the link budget at mmWave frequencies are *i*) shortening communication distance, *ii*) increasing antenna gain, and *iii*) increasing transmitted power. The former is often undesirable or impractical (e.g., satellite communications). Therefore, increasing antenna gain and transmitted power (while complying with regulatory standards) at the transmitter is the obvious solution to compensate for the additional path loss in the link budget at higher frequencies. Consequently, array antennas integrated with front-end electronics, providing high antenna gain and enabling digital beamforming, are considered critical components in future mmWave wireless communication systems. This thesis focuses on the integration of antennas and power amplifiers (PAs) in the transmitter arrays.

The fifth generation of mobile wireless technologies (5G) aims to achieve data rates up to 10 Gbit/s through the use of the lower end of the mmWave frequencies [4]. At these frequencies, multi-antenna systems with numerous integrated active antennas are necessary to overcome the substantial path loss between the base station and mobile user equipment; beyond-5G exploits even higher frequencies, i.e., above 100 GHz and up to 300 GHz [5], [6].

1.2 Design Challenges in Millimeter-Wave Wireless Communication

Energy-efficient integration solutions are needed to enable the 5G and beyond applications. Also, compact and cost-effective physical realization (so-called *building practice*) is required since mmWave integrated array antenna systems will employ many transceivers and active antenna elements [7]. It is desired for integrated front-end electronics to be confined within the cross-section of the antenna aperture or the sub-array of elements to enable modularity. Furthermore, considering the substantially reduced antenna footprint at mmWave frequencies and high level of integration with electronics, novel interdisciplinary co-design flows are demanded to address the complex interactions between the antenna radiation and mutual coupling (MC), linearity, energy efficiency, and heat dissipation of the transmitter. Furthermore, it is necessary to include the effects of antenna MC to evaluate the PA active load impedance. The challenge here is that the antenna array element impedance, i.e., the load seen by the PA, varies during beam scanning, which can significantly affect the power efficiency and output power of the PA [8], [9]. Accordingly, it is imperative to consider the antenna MC effects and PA nonlinearity through the PA-antenna co-design to achieve the theoretically possible optimal system performance of the integrated design.

Another complication is that the physical antenna ports in the integrated PA-antenna systems are not accessible. Thus, radiating antenna elements and their interconnected PAs cannot be

[1] In the spherical coordinate system, (r, θ, ϕ) gives the radial distance, polar angle, and azimuth angle.

characterized individually. The over-the-air (OTA) characterization becomes critical and the only viable approach. Characterizing the active integrated antenna (AIA) in anechoic chambers may suffer from measurement uncertainties due to probe misalignment or reflections from the chamber environment. Therefore, it may involve a complicated and time-consuming calibration procedure. More attention to details in calibration and measurement is needed compared to the OTA characterization of sub-6 GHz passive antennas.

The challenges in simulation, design, integration, physical realization, packaging, and validation are more involved for mmWave integrated antennas than for sub-6 GHz. Conventional circuit and antenna design techniques at the isolated component level are no longer applicable and can lead to suboptimal design and performance in the mmWave spectrum [10]. For instance, microstrip feed lines are commonly utilized in circuit and antenna design at sub-6 GHz frequencies due to them being affordable, low-profile, and having well-established characteristics. However, specific problems of microstrip lines start to appear when designing in the mmWave frequency range. To name one, the conductor and dielectric losses are proportional to the frequency. Also, microstrip lines with large areas or discontinuities can lead to spurious radiation effects that substantially impact the antenna radiation pattern or cause circuit crosstalk effects. Additionally, the choice of substrates can also decrease the antenna radiation efficiency due to dielectric losses [11]. Maximizing antenna efficiency and limiting interconnect losses are critical challenges in mmWave antenna design.

Three specific application domains are associated with the AIA designs in this research project: *space-borne communications*, *defense applications*, and *terrestrial cellular communications*. A commonly aligned list of system constraints tailored by the industrial partners of this project (Ericsson, RUAG Space, and Saab) has been used as the starting point of this work, which is summarized in Paper [**A**] and listed in Table 3.1.

1.3 Millimeter-Wave Active Integrated Antenna Technologies

Various solutions have been investigated to build cost-effective and energy-efficient AIAs for mmWave applications, such as *antenna-on-chip (AoC)*, *antenna-in-package (AiP)*, and *hybrid* integration design. The definition and overview of these solutions are introduced in this section.

Antenna-on-Chip

Antenna-on-chip (AoC) and system-on-chip (SoC) are low-cost, reliable, mass reproducible, and miniaturized. These characteristics promise affordable commercial wireless solutions; however, there are also design challenges. First, the complementary metal oxide semiconductor (CMOS) process is relatively cost-effective and the mainstream technology for digital circuits. Nonetheless, silicon substrates are not optimal for realizing efficient radiating properties due to their low resistivity (ρ = 1–20 Ω-cm) and high permittivity ($\varepsilon_r = 11.9$) [12]. Low resistivity results in Ohmic loss, i.e., heat dissipation. High permittivity and thick substrates trigger substrate modes, which can severely affect the antenna radiation pattern and generate surface waves in the sub-

strate. These surface waves can lead to issues with impedance mismatch and scan blindness in array systems. Several techniques utilized to enhance the AoC radiation efficiency are: (*i*) substrate thinning [13]–[15]; (*ii*) proton implantation [16]–[18]; (*iii*) micromachining [18], [19]; (*iv*) superstrate focusing [20], [21]; and (*v*) EM shielding by applying an artificial magnetic conductor (AMC) surface in a CMOS process [22]–[27].

There are other barriers in AoC design, e.g., the layout is dictated by the foundry-specific rules, and there are no provisions for AoC; therefore, resolving the design rule checking (DRC) errors is particularly troublesome. In addition, the packaging can significantly influence the AoC characteristics, such as radiation pattern and antenna impedance. It is not straightforward but essential to consider these effects in the design process [28], [29].

Antenna-in-Package

Currently, there is much interest in antenna-in-package (AiP) technology for 5G New Radio (NR) [30]. AiP can provide higher antenna gain and radiation efficiency thanks to a low loss substrate compared to AoC. Furthermore, the AiP solution enables a much shorter interconnect to the front-end circuit than a conventional discrete antenna. Shorter interconnects imply lower transmission losses, thus enhancing the transmitter's energy efficiency and the receiver's noise figure.

Similar to integrated AoC, one needs to design the AiP together with the front-end electronics in the initial system architecture phase for optimal results. Moreover, a well-confined EM environment in AiP is preferred so that the antenna performance is less susceptible to the presence of the package, printed circuit board (PCB) substrate, and metallic structures [31]. When jointly designing the AiP and the front-end electronics by implementing the circuit-antenna co-design methodology (see Section 3.1), one can take account of the coupling effects and crosstalk between the AiP and the front-end integrated circuit (IC) to achieve optimal designs.

Hybrid Integration Active Antenna

An antenna integrated with the front-end circuit, which is neither implemented in the packaging technology nor the IC back-end, is referred to as *hybrid integrated antenna concept*, or as *hybrid concept* for short [32]. In many AIA designs, the integrated system is either built on ICs or integrated through packaging. This type of integration is straightforward to design and assemble, with the least complexity; however, it also comes with design limitations, restraining the system performance of the integrated designs. For instance, AoCs and PCB antennas have intrinsically low to medium radiation efficiency and narrow bandwidth; on the contrary, slotted waveguide antennas have high radiation efficiency, but they are bulky and only have limited spaces for front-end circuit integration. It is challenging for PA-antenna integration designs of AoC, SoC, AiP, or system-in-package to satisfy the *system constraints* (Table 3.1) of the three application domains due to the aforementioned intrinsic limitations of the technologies. On the other hand, hybrid integration active antenna system solutions are particularly advantageous in

delivering custom design specifications by leveraging more degrees of freedom of integrating different technologies.

Common challenges in active integrated array antenna systems for 5G and beyond wireless communications include but are not limited to:

Challenge 1 *The size of the antenna element and array element spacing should be $\sim 0.5\lambda$ to avoid radiating grating lobes in the visible space, leading to physical size constraints for integrating electronics and manufacturing difficulties.*

Challenge 2 *Radiating elements of modern integration technologies such as antenna-on-chip (AoC) commonly suffer from low antenna gain and radiation efficiency (silicon substrates) as well as low output power and poor energy efficiency of integrated array transmitters. Typically, antenna gain <2 dBi and radiation efficiency <55% in Ka-band.*

Challenge 3 *Most active integrated antenna designs have additional lossy intermediate transitions and impedance matching circuitry between the radiating elements and power amplifiers.*

Challenge 4 *Integration is commonly conducted at the component level. The radiating elements and electronic components, e.g., power amplifiers, are designed independently from one another, assuming a typical 50-Ohm interface. This is generally different from the optimal interface impedance needed to maximize the power-added efficiency and output power.*

This research aims to develop new integration solutions to address these challenges.

1.4 Scientific Contributions of the Thesis

Six original scientific contributions (SCs) of this thesis are:

SC 1 A new interdisciplinary co-design methodology for integrated active array antennas that accounts for the crosstalk effects between the active integrated circuits and the radiating antennas is proposed. It enables an antenna-integrated transmitter with maximized power efficiency and linearity over a wide frequency band (25.8–29.6 GHz) as demonstrated in Paper [**A**] and [**F**] (*primary contribution*). The achieved peak *overall power efficiency*[1] of the PA-integrated active antenna at the 1 dB compression point is 40%.

SC 2 A design of a high-power, high-efficiency K-band GaN HEMT power amplifier-integrated active antenna element by applying the proposed co-design methodology is presented. The *overall power efficiency*[1] of such an integrated PA-antenna module can be enhanced

[1] including the PA drain efficiency and antenna radiation efficiency

by directly matching the PA output to the optimal impedance, which is typically very different from the standard 50 Ω and complex-valued ($Z_{opt} = 17 + j46$ for the GaN HEMT used in this work); presented in Paper [**B**] (*primary contribution*).

SC 3 The active integrated unit cell (AIUC) design approach and a new performance metric for active integrated array antennas, active scan element pattern (ASEP), are proposed, extending the conventional infinite array unit cell approach for passive array antennas to active scenarios to account for the nonlinearity and nonreciprocity of the co-integrated PAs. The AIUC, simulating the EM environment of an infinite array antenna element, is experimentally verified by the infinite array waveguide simulator technique; presented in Paper [**E**] (*secondary contribution*).

SC 4 A design of a mmWave high-efficiency AIUC with improved bandwidth with respect to the design in Paper [**B**] and wide scan range (FBW: 11% as the *overall power efficiency* $\geq$20%, scan range of $\pm 55°$ in the E-plane and $\pm 40°$ in the H-plane) is proposed. The integrated PA MMIC is custom-developed in a GaAs process[1], and the contactless interconnect is implemented at the PA-antenna interface for enhanced bandwidth and power efficiency with 22 dBm saturated power, presented in Paper [**F**] (*primary contribution*).

SC 5 A new scattering parameters re-normalization technique for the analysis of mutual coupling effects in highly integrated transmitter arrays is proposed. It extends the applicability of the conventional S-parameters approach used to quantify the mutual coupling effects in passive antenna arrays to active integrated (generally multi-port) antenna array scenarios; presented in Paper [**C**] (*primary contribution*).

SC 6 A study of design trade-offs between various design parameters by optimal load matching with three design examples, emphasizing the benefits of the direct impedance-matching technique for maximizing the power-added efficiency, saturated power, or PA linearity, are presented in Paper [**D**] (*primary contribution*).

1.5 Thesis Outline

The scope of this thesis is illustrated in Fig. 1.1, and the thesis outline is as follows. The AIA design considerations are discussed in Chapter 2. Chapter 3 presents the proposed interdisciplinary co-design methodology and the integration method for PA-integrated active antenna (PAIAA) elements. The mutual coupling effects in highly integrated AIAAs and the design examples of optimal PA loading for different design parameters are presented in Chapter 4. The active integrated unit cell (AIUC) and the proposed characterization technique for AIUCs—*active infinite-array waveguide simulator* are investigated in Chapter 5. The design example of a broadband AIUC integrating the custom-designed PA MMIC is introduced in Chapter 6. The conclusion and future work are discussed in Chapter 7.

[1] WIN Semiconductor PIH1-10 4 V GaAs *p*HEMT MMIC Technology [33]

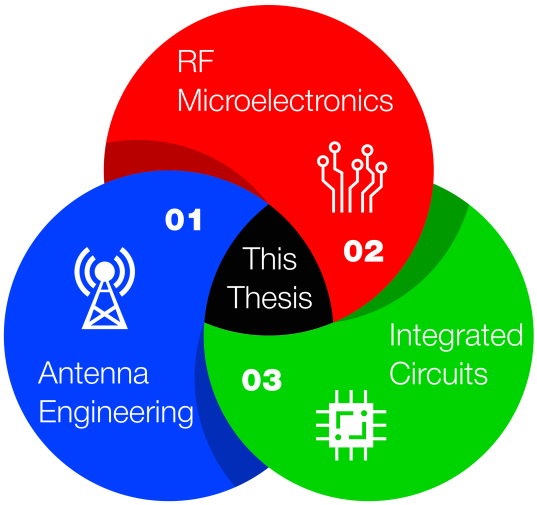


Figure 1.1: The scope of this thesis.

CHAPTER 2

STATE-OF-THE-ART DESIGN METHODS FOR ACTIVE INTEGRATED ANTENNAS

This chapter gives an overview of different integration concepts for circuit-antenna design and modeling, i.e., *conventional* individual component-level design, *high integration*, and *deep integration*. The state-of-the-art active integrated antenna design examples based on these methods are summarized, and their advantages and disadvantages are discussed.

2.1 Overview of Integration Concepts

There are various definitions of the AIA in the literature [34]–[36] that describe the levels of integration for the active antenna system, as shown in Table 2.1. Conventionally, the antenna is integrated into the front-end electronics by simply interconnecting the components, and the boundary between the sub-systems is distinct. Thus, they are generally designed and analyzed by two teams of specialists, i.e., circuit and antenna designers individually, as shown in Figure 2.1a. The individual teams need to transform the interface impedance to an equal value (generally 50 Ω) to minimize the mismatch between the sub-systems, which is generally realized by impedance matching networks (IMNs). These sub-systems are well-isolated because of the IMNs; however, the footprint of conventional designs becomes bulky, and the power losses increase due to these networks. Therefore, such a conventional 50 Ω design is not an optimal candidate for large-scale arrays in mmWave frequency applications.

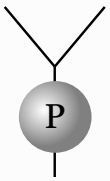
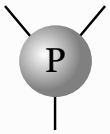
IMNs are obviated in the *high integration* approach to avoid the aforementioned drawbacks. Thus an active antenna of *high integration* can have a smaller form factor and higher power efficiency than the conventional active antennas, especially at high frequencies and in wideband applications. Consequently, one needs to define an arbitrary interface impedance between the sub-systems due to the absence of IMNs. The optimal system performance can be attained through

Figure 2.1: (a) A traditional 50-Ω interface/boundary between circuit and antenna designers and (b) circuit-antenna integration with arbitrary interface impedance.

a customized interface impedance, which is typically not 50 Ω. Hence, it is necessary to exploit an interdisciplinary co-design methodology to determine the optimal interface impedance and jointly optimize the active component and the radiating element for this impedance. This methodology must take all the critical interaction effects into considerations, such as *intra-element* and *inter-element* MCs (addressed in Section 4.1), and hence realize optimal system performance.

The designers can have a higher degree of freedom in AIA designs by adopting the *deep integration* concept. *Deep integration* [36] incorporates the active component into the radiating

Table 2.1: Different integration levels of circuit-antenna designs and their advantages and disadvantages.

Conventional 50Ω design	High Integration	Deep Integration
		
+ Well-isolated sub-systems and components + Well-established design approach – Bulky design and high power losses – Not well-suited for mmWave applications and large-scale arrays	+ Custom interface impedance (eliminate output IMN) + Smaller form factor and reduced power losses – Requires interdisciplinary co-design	+ Consolidated design, active devices unite with radiating elements + Higher degree of freedom in co-optimization – Involved integration level – Challenging to implement – High risk of self-oscillation

element (inseparable) and consequently can provide a design with the smallest form factor. However, this type of integrated circuit-antenna module is complex and challenging to analyze since it requires joint EM-circuit analysis. That is, antenna designers need to possess interdisciplinary skills and knowledge, such as knowledge of monolithic microwave integrated circuits (MMICs) design and process, to be able to design deeply integrated AIA designs. Practical implementation challenges are formidable due to a lack of suitable manufacturing processes and a high risk of self-oscillation caused by poor isolation between the components.

PA-antennas interconnected by conventional IMNs with large impedance transformation ratios often experience noticeable insertion loss and limited bandwidth [37]–[40]. Various factors can contribute to the insertion loss at the interface between sub-systems, such as metal loss, dielectric loss, substrate conductivity (considerable contributor in silicon substrates), and radiation loss. Radiation loss results from the stray radiation of microstrip lines. The stray radiation can affect the antenna radiation pattern, result in undesired crosstalk, and deteriorate energy efficiency and thermal dissipation. The effect of IMNs with different insertion losses and bandwidths on PA's maximum power-added efficiency (PAE) was studied in [40], demonstrating that in most designs, where the length of the matching network varies from 0.8–1.7λ_g[1], experience at least 30% PAE reduction compared to the maximum. This study shows that by using direct integration, i.e., *high integration*, it is possible to improve the PAE up to 10% over a 5% frequency bandwidth by reducing the insertion loss and thus increasing the power efficiency.

In conclusion, although providing adequate isolation between sub-systems or discrete components, the conventional integrated antenna is large and lossy and, therefore, not well-suited for mmWave large-scale active arrays. On the other hand, deeply integrated active antennas can likely provide the smallest form factor and most negligible transition loss. Despite that, the involved integration level also suggests a high risk of system self-oscillation due to poor isolation between sub-systems and the fact that it is more challenging to analyze the consolidated AIA correctly. The *high integration* concept represents a compromise in terms of form factor, power efficiency, and manufacturability. Hence, the *high integration* concept is adopted in this research.

The primary challenge in high integration power amplifier-integrated active antenna (PAIAA) designs is determining the optimal PA-antenna interface impedance. On the one hand, high-power PAs typically prefer a load of low resistance and inductance to resonate out the output parasitic capacitance for maximum PAE and delivered power. Nevertheless, the choice of semiconductor technology dictates the size of bandgaps and the breakdown voltage of transistors [37], [39], which constrains the load line and thus the optimal load resistance[2]. On the other hand, a higher antenna input resistance is preferred high for attaining high radiation efficiencies, such as 50 Ω or 75 Ω that are the typical characteristic impedance values of transmission lines. The optimal load impedance of the two sub-systems is profoundly distinct. Consequently, it is implausible to find an arbitrary interface impedance to attain peak performance for both sub-systems. Hence, a trade-off study is required to determine the optimal interface impedance to

[1] λ_g is the guide wavelength of the substrate.

[2] The typical optimal load resistance of a PA is around 18 Ω for GaN technology and around 5 Ω for CMOS technology.

meet the targeted design goals.

2.2 State-of-the-Art PAIAA Design Examples

Previous studies of PAIAA designs were reported in [41]–[53]. For instance, [44] presented a C-band GaN-HEMT PAIAA design, achieving a maximum output power of 38 dBm and a peak PAE of 59%. The PA and antenna were interconnected via a harmonic tuning circuit[1] and a IMN. Although the design had good thermal management capabilities, the integrated antenna size was rather bulky ($1.9\,\lambda \times 1.9\,\lambda \times 2.1\,\lambda$). A monolithic 24 GHz receiver integrated with an on-chip folded dipole antenna was manufactured in a 0.8 µm silicon germanium (SiGe) heterojunction bipolar transistor (HBT) process [46]. This design was compact in terms of wavelength ($0.17\,\lambda \times 0.18\,\lambda$). However, the integrated on-chip radiator had merely -2 dBi gain. A W-band PAIAA design in silicon technology was investigated in [45]. The antenna size was $0.4\,\lambda \times 0.4\,\lambda$. However, its peak PAE was merely 6.4%, and the measured active antenna gain[2] was 9.4 dBi, while the dipole antenna gain was -8.5 dBi. Song et al. presented a Ka-band AIA in package (AIAiP) [47]. The antenna was implemented on a PCB and integrated with an MMIC amplifier in a GaAs process. The antenna and amplifier were assembled within a ceramic package and interconnected by bond wires. The size of the AIAiP was $0.8\,\lambda \times 0.8\,\lambda$, and the design demonstrated an active antenna gain[2] of 18.9 dBi at 35 GHz; however, the PAE and transducer gain were not documented.

Integrated solutions implemented in AoCs and AiPs are cost-effective at higher mmWave frequencies (above 60 GHz). At lower frequencies, on-chip implementation is challenging since a relatively large physical chip area is needed. Therefore, AoCs at frequencies below 60 GHz become expensive and may even not be manufacturable due to the restrictions of the process. For example, the maximum deliverable reticle size of the process can be in the order of 10 mm $\times$ 10 mm, which is approximately $1\,\lambda \times 1\,\lambda$ at 30 GHz.

As mentioned in Section 1.3, other design challenges may occur depending on the implemented technology (e.g., AoC or AiP). These technology challenges and their solutions are outside the scope of this work and thus not discussed.

A summary of the state-of-the-art PAIAA designs is listed in Table 2.2, in which these state-of-the-art examples represent the common challenges as well as the ones associated with the implemented solutions, e.g., AoC, AiP, or hybrid. Among the plethora of studies on PAIAAs, a PA-antenna co-design methodology for achieving optimal PAIAA designs that correctly accounts for the nonlinear behavior of transistors and the MC effects of antennas is lacking. Such an interdisciplinary design methodology is introduced and discussed in Chapter 3.

[1] Harmonic tuning circuits are used to shape the drain waveform of the second and third-order harmonics to enhance the PAE and output power.

[2] Active antenna gain is defined in Section 3.3.

Table 2.2: State-of-the-art PAIAA examples and common design challenges.

Ref	Implemented solutions	Freq [GHz]	Challenges
[41]	Hybrid, Conventional	2	AIA size not suitable for array applications
[54]	Hybrid, high integration	2.14	AIA size not suitable for array applications, challenging to precisely control the dual feed to Doherty PA
[55]	Hybrid, deep integration	3	Challenging to implement and troubleshoot, high risk of self-oscillation
[51]	Hybrid, high integration	3	Radiation pattern distorted due to the proximity of the active device
[50]	Hybrid, high integration	3.5	Only applicable to 1D array due to size ($0.9\,\lambda \times 0.5\,\lambda$)
[56]	Hybrid, high integration	3.5	AIA size not suitable for array applications ($1\,\lambda \times 1\,\lambda$)
[49]	Hybrid, high integration	3.65	Only applicable to 1D array due to size ($1.1\,\lambda \times 0.6\,\lambda$), poor antenna gain
[43]	Hybrid, conventional	4.15	AIA size not suitable for array applications
[53]	Hybrid, deep integration	5	AIA size not suitable for array applications ($0.8\,\lambda \times 0.7\,\lambda$), low PAE
[44]	Hybrid, conventional	5.8	AIA size not suitable for array applications, not co-designed, not optimized via direct match
[42]	Hybrid, conventional	7.25	AIA size not suitable for array applications, narrowband (impedance bandwidth$<$1%)
[46]	AoC, high integration	24	Low antenna gain (-2 dBi), narrowband (impedance bandwidth $<$3%)
[57]	AoC, high integration	24	Low efficiencies (simulated PAE$<$25.6%, $\eta_{\text{rad}}<60\%$)
[47]	AiP, conventional	35	AIA size not suitable for array applications ($0.8\,\lambda \times 0.8\,\lambda$), Γ_{ant} affected by package size, not optimized via direct match, not co-designed
[48]	Hybrid, conventional	38	AIA size not suitable for array applications ($1\,\lambda \times 1\,\lambda$), model accuracy impacts the performance
[58]	AoC, conventional	60	Low η_{ant}, not optimized via direct match, without co-design
[45]	AoC, high integration	79	Low η_{ant} ($G_{\text{ant}} = -8.5$ dBi)
[52]	AoC, deep integration	146	Poor power efficiency, high risk of self-oscillation

2.3 Conclusion

The *high integration* (direct integration) method can significantly improve the power efficiency of antenna-integrated PAs by directly matching the antenna impedance to the PA optimal load impedance without using an intermediate lossy impedance-transforming circuitry. To enhance the system performance (e.g., PAE and active antenna gain) and ensure no self-oscillation, a circuit-antenna co-design methodology that accounts for the antenna port mutual coupling effects, circuit crosstalk, and amplifier nonlinearity is in demand.

CHAPTER 3

CO-DESIGN METHODOLOGY

A new interdisciplinary antenna-circuit co-design flow for active integrated antennas and array antenna designs is proposed in this chapter. A design example of active integrated antenna elements demonstrates a peak *system power efficiency*[1] of 50% by applying co-design and direct integration, in which the state-of-the-art solutions[2] typically have less than 15%.

3.1 PA-Antenna Joint Design

Joint Optimization

The initially proposed preliminary PA-antenna co-design flow in Paper [**A**] is generally applicable to PAs developed using commercially available off-the-shelf transistors. Therefore, this design flow is simplified due to limited degrees of freedom in PA designs, i.e., fixed transistor size suggests unchangeable maximum power gain, saturated power, and thus untunable optimal load impedance of such a device. Hence, custom on-chip PA designs are inevitable for more design flexibility and optimal integration. A joint optimization design flow for highly integrated PA-antenna designs is proposed, taking into account both the PA design and subsequent antenna integration to determine an optimal loading condition based on design specifications, as shown in Fig. 3.1. The design flow starts from the design specification highlighted in Table 3.1 and the selection of a suitable IC technology, and PA topology, as detailed below.

[1] Including power amplifier drain efficiency and antenna radiation efficiency.

[2] Doherty amplifiers and other amplifiers that require additional linearization techniques are disregarded.

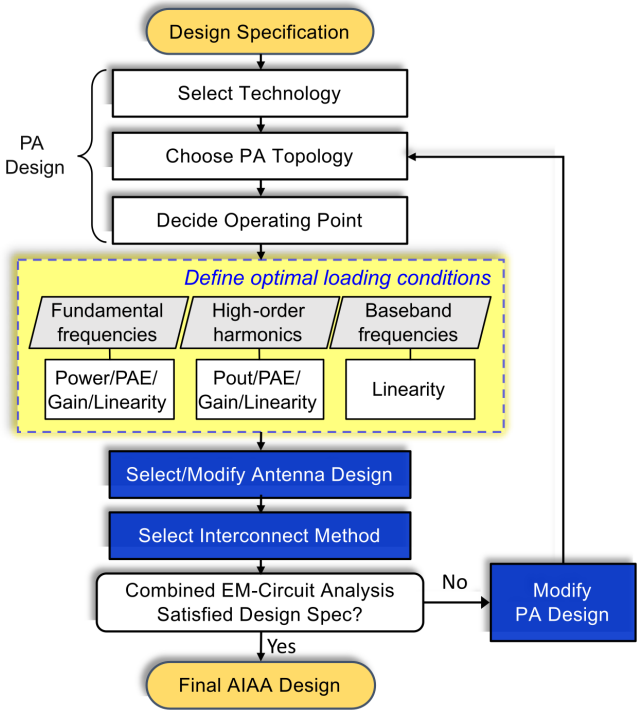


Figure 3.1: Joint PA-antenna design flow for highly integrated systems.

Select Technology

The semiconductor technology's capabilities bound the operating frequency and the peak output power of the front-end IC devices. Silicon-based technologies are known to be relatively affordable to manufacture and can handle complex (multi-dimensional) designs owing to their multilayer process. In particular, CMOS with improved transistor core technologies are seen as competitive low-cost PA and SoC solutions, even for circuits and systems design above 100 GHz [39], [60]; SiGe HBTs have improved achievable gain and cutoff frequency (above 100 GHz), combining the high-frequency performance and a low-cost, functional integration comparable to CMOS [60]. However, silicon has diminutive peak output power, particularly in the mmWave range [61]; this is because the peak output power of semiconductor devices is intrinsically confined by the technology's breakdown voltage [7]. On the other hand, III-V compound semiconductors such as Gallium Arsenide (GaAs) and Gallium Nitride (GaN) have peak output powers an order of magnitude higher than the conventional silicon-based materials due to their large bandgaps and high breakdown voltages [39]. GaN and GaAs technologies also have higher PAE than CMOS devices due to their high maximum power density. Furthermore, III-V technologies can enhance the link distance significantly, while CMOS and SiGe processes suffer from limited output power and higher noise [62]. Fig. 3.2a and Fig. 3.2b summarize the saturated power and the peak PAE for all reported PAs and transmitters since 2000 over frequency in various semiconductor technologies till the present day [61], which underlines the importance of III-V

semiconductors for achieving high-power and energy-efficient mmWave transceivers.

Consequently, the integrated PAs in this thesis are designed in GaN and GaAs technologies for their promising high power and high PAE.

Choose PA Topology

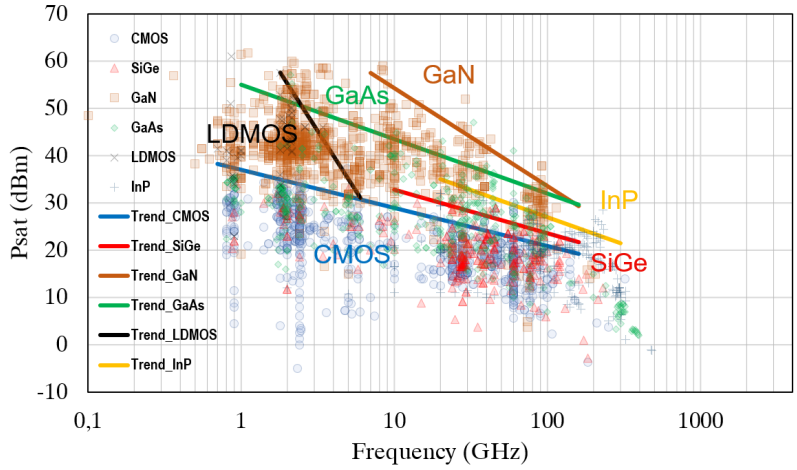
The transistor size in terms of the gate finger width and the number of fingers is proportional to the saturated power and inversely proportional to the power gain [63], which is usually a design trade-off between various aspects such as the link budget and PAE. The device size can be decided once an adequate trade-off between output power and device gain has been made. Additionally, the size of the transistors influences the PA optimal load impedance, which can be exploited as a degree of freedom in PAIAA design and optimization. In this case, the antenna impedance is used to synthesize the PA optimal load and maximize the radiation resistance and antenna efficiency.

Table 3.1: The aligned system constraints derived from three mmWave application domains (*space-borne communications*, *defense applications*, and *terrestrial cellular communications*) for integrated array antennas at mmWave frequencies [59].

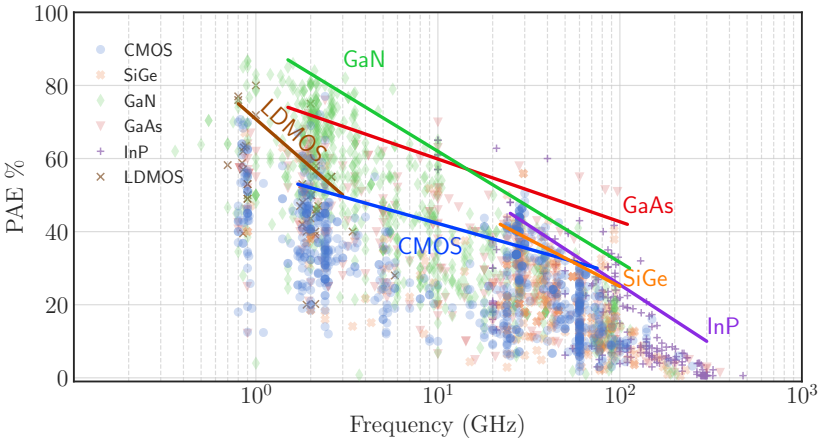
Design Parameters	Constraints
Array aperture area	10–100 λ^2
Array configuration	planar*, $\sim 0.5\lambda$ spacing
Radiating element	dual-polarized
Frequency band	20–40 GHz (not continuous)
Bandwidth	5–10%
Instantaneous bandwidth	1–5%
Beamforming	digital
Scan angle	$\pm 60° \times \pm 60°$ (EL$\times$AZ)†
Peak output power per element	15–25 dBm
Isolation between PAs at output	-15 dB
Noise figure	5–7 dB
Total power efficiency	25%

* Planar array in rectangular grid.

† EL: the elevation angle, AZ: the azimuth angle.



(a)



(b)

Figure 3.2: (a) The saturated power and (b) the peak PAE of all reported PAs and transceivers since 2000 as a function of the frequency [61], highlighting the importance of III-V technologies in mmWave 5G and beyond wireless applications.

The number of active devices in series and parallel affects the PAE, power gain, and saturated output power. PAs with more stages (devices in series) generally have higher device gain; however, they also suffer from lower drain efficiencies due to higher direct current (DC) consumption from biasing the transistors. On the other hand, more parallel devices can increase the peak output power through power combining, providing the loss from the power combiner is lower than the increased power from the parallel transistors. The targeted output power is 15–25 dBm in this research (Table 3.1), and a moderate gain (15–20 dB) is needed for enhancing the PAE. Hence, a two-stage PA design is proposed in the final design example of this research, where a single transistor is implemented at each stage since GaN- and GaAs-based transistors have sufficient power density to meet the targeted output power.

Decide Operating Point

The operating point of the transistors defines the amplifier class. Transistors are generally biased in the middle of the load line for class A amplifiers, which gives the most linear and high gain behavior. However, PAE is a critical performance metric in communication blocks, particularly in 5G and beyond-5G wireless communications. Techniques for attaining higher PAE and calibrated linearized behavior, e.g., Doherty PAs and digital pre-distortion (DPD), have drawn considerable research attention. Nonetheless, despite delivering enhanced efficiency and improved linearity, those techniques are of high complexity and costly if deployed in massive MIMO (multiple-input and multiple-output) scenarios.

Class AB amplifiers are considered in this thesis for their relatively high power efficiency and adequate linearity without the need for any complex and computationally expensive linearization techniques.

Define Optimum Loading Conditions

As shown in Fig. 3.1, the PA loading condition at the fundamental, high-order harmonics (at the transistor output), and baseband frequencies (at the biasing ports) all contribute to the characteristics, such as saturated output power P_{sat}, operating power gain G_P, PAE, and linearity. By varying the PA load impedance, i.e., the impedance of the integrated antenna at the fundamental and high-order harmonic frequencies, while keeping the PA design unchanged, the integrated PA-antenna could virtually attain a maximized system efficiency, significantly improved linearity, or an in-between trade-off solution [64] (see Sec. 4.2). Analogously, the system linearity can also be substantially improved by proper loading and termination in the baseband [65].

The terminology used to define PA load impedance/loading conditions:

- Fundamental load: The PA loading condition at the fundamental frequency f_0, i.e., antenna impedance at this frequency.
- Harmonic load: The PA loading conditions at higher-order harmonic frequencies $2f_0$, $3f_0$, ..., i.e., the antenna impedance at those harmonic frequencies.

The load-pull technique is widely practiced in analyzing the large-signal behavior of amplifiers, i.e., when operating in the nonlinear regime [37], [63]. The amplifier optimal loading condition for specific design criteria can be determined by varying the load impedance in simulations or measurements over an extensive range of complex values. In this research, the PA load represents the antenna impedance directly interfaced with the amplifier output, and the load-pull results contribute to the choice of optimal interface impedance, as shown in Fig. 3.1. The harmonic loads can significantly affect the operation of power amplifiers [66]; therefore, the optimization of the loading conditions at those frequencies is also taken into consideration in the antenna design process.

Select Antenna Design

The antenna type is dominated by the optimal load impedance attained in the previous step due to the absence of intermediate impedance matching networks at the interface between antenna and front-end circuit. Most PA performance metrics (e.g., P_{sat}, G_P, and η_{D}) peak when the transistor is loaded with a complex-valued load due to the parasitic capacitance at the output. Choosing an appropriate antenna type can simplify the direct integration process and obtain wideband performance.

Select Interconnect Method

The interconnection between PAs and antennas can impact the isolation, power efficiency, form factor, assembly complexity, and stability of the PA-antenna integration. For instance, wire bonding is commonly utilized in interconnecting antennas and electronics. However, wire bonding is no longer an optimal option at high frequencies such as W-band and D-band since the length of the bond wire turns into a very sensitive and difficult-to-control parameter. The inductance varies drastically as the bond wire length changes, which can complicate impedance matching. Additionally, the bond wire is seen as a radiator for spurious radiation, which is not desired in communication systems [32].

Nonetheless, wire bonding is implemented to *directly* interconnect the antenna and the PA in the first proof-of-concept due to its accessibility in prototype assembly (Sec. 3.2). A contactless transition is proposed to replace the bonding wire to enhance the bandwidth; this interconnection method is less frequency-dependent than bonding wires and can provide a broader frequency band transition, as demonstrated in the final design (Chapter 6).

Combined EM-Circuit Analysis

Next, after the first iteration in the PA-antenna joint design flow, it is imminent to analyze the integrated design with a more rigorous approach in a combined circuit-EM co-simulation environment. The proposed PA-antenna joint optimization is an iterative process. By leveraging the interdisciplinary knowledge of PA and antenna designs, one can optimize the integrated active array antennas design parameters (Table 3.1) by making design trade-offs at the system level.

The signal and DC feed lines, and the transistor model in the PAIAA design example are numerically analyzed in Keysight Advanced Design System (ADS) [67]. In contrast, the passive components and the radiating element are simulated in the combined EM-circuit solver, as shown in Fig. 3.3b. The nonlinear behavior of active components cannot be analyzed in EM simulators. Therefore, the combined EM-circuit analysis is required to take into account these nonlinear effects in large-signal analyses, which can lead to suboptimal system performance if overlooked in the design phase. For instance, the third-order intercept point (TOI) indicates the vulnerability to intermodulation distortion (IMD) when two or more signals are fed to the nonlinear device. Implementing the EM-circuit joint analysis in AIA designs can ensure the TOI is optimized to the highest level to prevent the system from suffering from distortion.

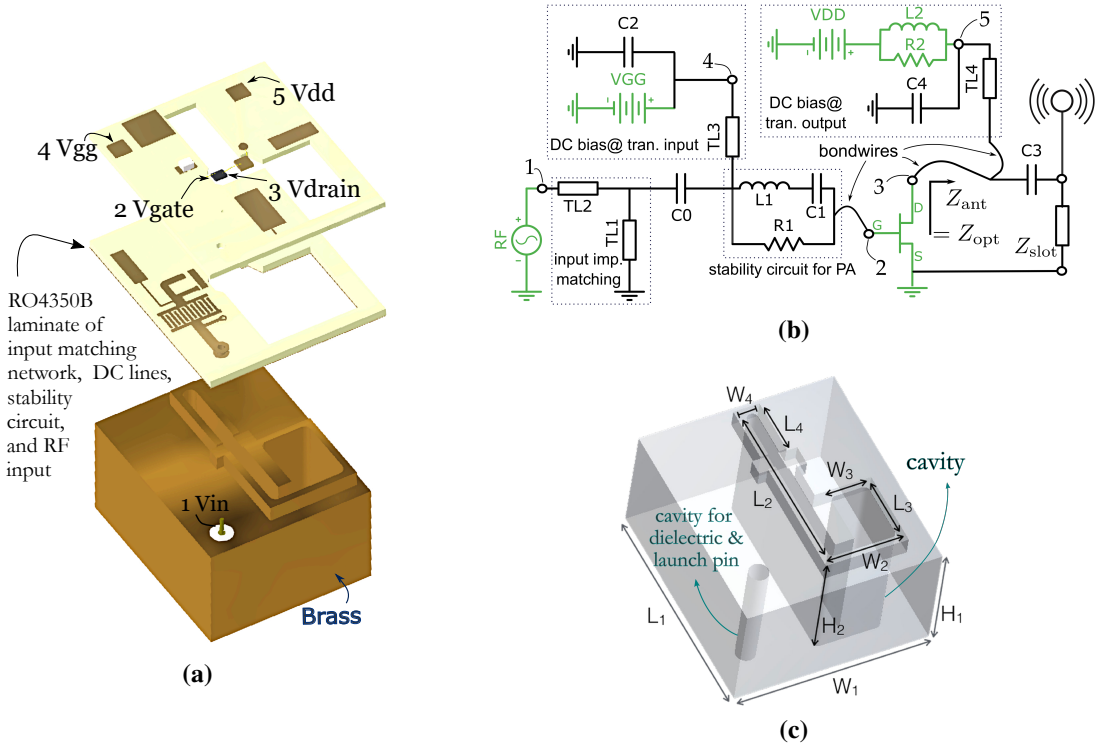


Figure 3.3: (a) The EM model and (b) the circuit model of the PAIAA design example. Five ports of the PA-IAA model used in the co-design are denoted: $V_{in}, V_{gate}, V_{drain}, V_{gg}, V_{dd}$. Implementing direct optimal impedance match to the PA for maximized PAE and obviating the use of (lossy) IMNs. The transistor die is integrated via a bond wire over the radiating slot. Green components are modeled in the circuit solver. The others are modeled in the full-wave EM solver. (c) PAIAA design and the design parameters (see Table 3.2).

Conventionally, there is only one port per antenna element in passive antennas that represents the excitation port. In multiport PAIAA designs, the radiating structure and integrated active devices must be jointly analyzed. It is essential to accurately analyze the coupling mechanism between ports since, as the multiport PAIAA elements are used in an antenna array, coupling effects may exist between these ports. However, the coupling mechanism of multiport AIA arrays is more complicated than that of passive antenna arrays (see Chapter 4). The reflected or coupled power waves in an AIA array can alter the PA load impedance and thus the system characteristics or give rise to undesired feedback that affects the system stability [8].

This PAIAA example is a five-port circuit-antenna integrated design. The combined EM-circuit solver is interconnected by five single-mode ports between the circuit and the EM model, as shown in Fig. 3.3b and Fig. 3.3a. Multiple iterations are required before the co-optimized PAIAA design satisfies the design specification, such as adjusting the DC biasing of the transistor to improve the PAE or output power or modifying the antenna design to increase the radiation efficiency without compromising the PAE.

The PA in [45] was assumed to be a metallic plate in the EM solver, thereby neglecting the dielectric effect and approximating the OTA coupling behavior in the vicinity of the transition

between the PA and the dipole antenna. In this design example, the dielectric substrate, the bonding pads, and the metallic back cover of the transistor die are considered in the EM model. The bond wires used to excite the radiating element (from the drain pad across the radiating slot) and interconnect other circuitry components are also included in the model, as shown in Fig. 3.4.

3.2 Design Example: PA-Integrated Active Antenna

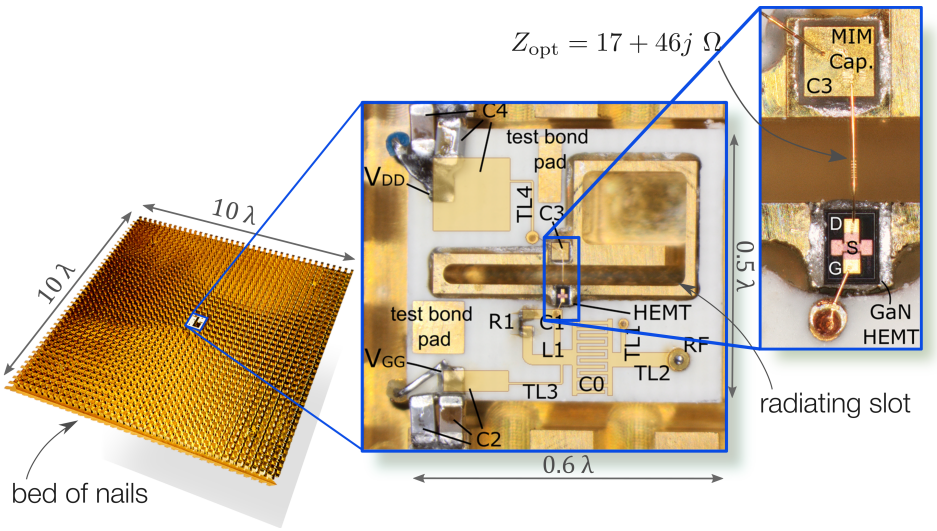


Figure 3.4: The PAIAA element operating at 20 GHz center frequency placed in a bed of nails, which is used as a ground plane with minimum edge effects for OTA characterization. The parameters of the radiating slot are shown in Table 3.2 and Fig. 3.3c. The shown circuitry corresponds to the circuit model in Fig. 3.3b, in which the translucent part is embedded in the middle layer of PCB laminate.

The PAIAA design example is co-optimized and verified in the combined EM-circuit analysis. The radiating element is directly integrated into the PA via a bond wire across the radiating slot, as shown in Fig. 3.4. The IMN is obviated in the interconnection at the PA and antenna interface to reduce the form factor and insertion loss. In conventional integration designs such as [44], the IMN and harmonic tuning circuitry were utilized to transform the impedance to 50 Ω and to improve the PAE by terminating the higher-order harmonics with short-circuit or open-circuit. Those circuitries enlarged the design footprint, making it inapplicable in array scenarios ($1.9\,\lambda \times 1.9\,\lambda \times 2.1\,\lambda$). Hence, in this PAIAA design, both the IMN and harmonic termination circuitry are absorbed in the antenna design.

The peak PAE and the fundamental output power of PAs are affected by the second- and third-order harmonics drain waveform shaping [68], [69], of which the efficiency can be treated as a function of higher-order harmonic impedances. In general, a maximum PAE requires harmonic short or open terminations at the PA output [68]. In this design, the antenna impedance at the second-order harmonic shows[1] $|\Gamma_D(2f_0)| \geq 0.96$ ($S_{11}^{2f_0} \simeq -0.3\,\text{dB}$) and $\angle\Gamma_D(2f_0)$ within 22.5° of

[1] $\Gamma_D(f_0)$: The reflection coefficient seen looking toward the radiating slot at f_0.

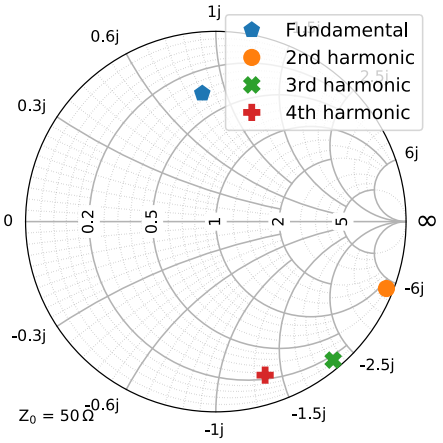


Figure 3.5: Simulated impedance of the radiating slot antenna element at the fundamental frequency (20 GHz), second (40 GHz), third (60 GHz), and fourth (80 GHz) harmonics.

an open circuit; at the third-order harmonic, the antenna impedance is $|\Gamma_D(3f_0)| \geq 0.95$ ($S_{11}^{3f_0} \simeq -0.4\,\text{dB}$) and $\angle\Gamma_D(3f_0)$ within 50° of an open circuit, as shown in Fig. 3.5. A peak power efficiency of 49.5% can be achieved theoretically with this harmonic termination[1]. At least 3% reduction in PAE can be expected if the higher-order harmonics are not terminated appropriately. In a less linear PA, the reduction in efficiency can be even worse.

The PAIAA prototype consists of a Qorvo TGF2942 GaN HEMT, a Rogers RO4350B multilayer PCB laminate for the PA circuitry, and a CNC-milled metallic radiating structure. For direct PA-antenna impedance matching, a cavity-backed slot radiator is selected, and a stub ($W_3 \times L_3 \times H_2$) is appended to the extremity of the slot ($W_4 \times L_2 \times H_2$) to alter the radiation impedance (Fig. 3.3c). The values of the impedance tuning parameters $H_2, L_2, L_3, L_4, W_2, W_3, W_4$ are listed in Table 3.2, in which $L_1, W_1,$ and H_1 indicate the PAIAA element dimensions.

Table 3.2: Geometrical parameters (unit: mm).

L_1	L_2	L_3	L_4	W_1	W_2	W_3	W_4	H_1	H_2
9.1	7.3	3.1	3.2	7.5	3.4	2.2	0.6	5.4	5.0

3.3 Experimental Characterization

The calibration and measurement setup and the relevant reference planes are presented in Fig. 3.6. The PAIAA is connected to an Agilent E8363B PNA network analyzer and DC-powered by a Rohde & Schwarz HMP4040 power supply. A pre-amplifier is used to increase the input power to the desired range (−10 dBm to 25 dBm). The reference plane for the received power ($P_{\text{rx,pna}}$)

[1] Including the PA drain efficiency and antenna radiation efficiency.

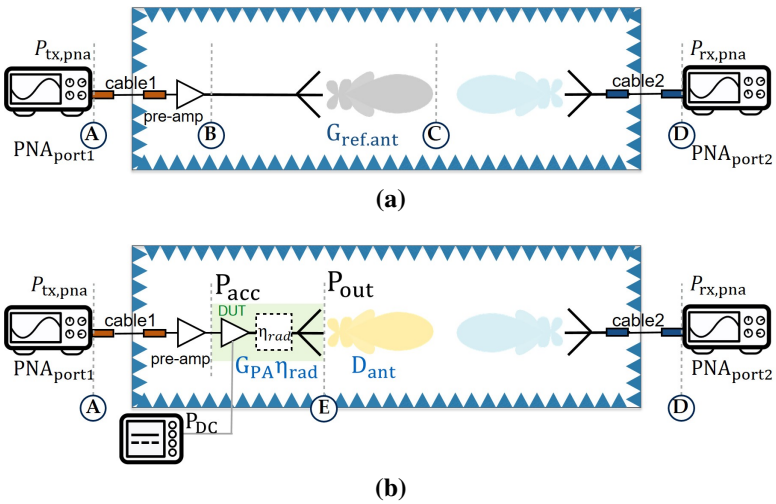


Figure 3.6: (a) Calibration with the reference antenna. (b) Measurement setup for characterizing the active antenna gain and power efficiency.

and the input available power ($P_{\text{tx,pna}}$) of the network analyzer, and the power accepted (P_{acc}) and radiated (P_{out}) by the AIA are denoted in Fig. 3.6b. The most important PAIAA performance metrics in this research are listed below:

Amplifier Transducer Gain [70]

$$G_{\text{PA}} = \frac{\text{the average power delivered to the load}}{\text{the average power available at the input}} = \frac{P_{\text{del}}}{P_{\text{acc}}}. \tag{3.1}$$

Power-Added Efficiency

$$\text{PAE} = \frac{P_{\text{del}} - P_{\text{acc}}}{P_{\text{DC}}}, \tag{3.2}$$

where P_{DC} represents the DC power consumption of the active device.

Drain Efficiency

$$\eta_D = \frac{P_{\text{del}}}{P_{\text{DC}}}. \tag{3.3}$$

Power Efficiency

$$\eta_a = \frac{P_{\text{out}}}{P_{\text{DC}}} = \frac{P_{\text{del}}\eta_{\text{rad}}}{P_{\text{DC}}}, \tag{3.4}$$

where η_{rad} represents the antenna radiation efficiency.

Active Antenna Gain [71]

$$G_{\text{AIA}} = G_{\text{PA}} G_{\text{ant}}, \tag{3.5}$$

where G_{ant} is the antenna gain of the integrated radiating element.

The PAIAA prototype (Fig. 3.3) is characterized experimentally over-the-air in the anechoic chamber at Chalmers. The characterization procedure is described below.

Calibration (Fig. 3.6a): This is the calibration to find the "*path gain*" G_{path}, including cable losses, pre-amplifier gain, and path loss. The calibration planes are in the reference plane B and C. The measurement is conducted with a standard gain horn antenna as the receiving antenna (port 2, PNA) and a reference antenna (with known antenna gain $G_{\text{ref.ant}}$) as the transmitting antenna. A pre-amplifier is connected before the reference antenna (port 1, PNA) to increase the input power to the -10 dBm to 25 dBm range. The path gain is calculated from

$$G_{\text{path}} = |S_{21}|^2_{\text{ref}} / G_{\text{ref.ant}} \ , \tag{3.6}$$

where $|S_{21}|_{\text{ref}}$ is the measured transmission coefficient from port 1 to port 2 (reference plane A and D).

Measurement (Fig. 3.6b): The active antenna gain and power efficiency of the PAIAA are characterized in this step. The reference antenna used in the calibration is replaced with the device under test (DUT). The active antenna gain of the DUT is obtained by

$$G_{\text{AIA}} = G_{\text{PA}} \eta_{\text{rad}} D_{\text{ant}} = |S_{21}|^2 / G_{\text{path}} \ , \tag{3.7}$$

where D_{ant} is the antenna directivity at broadside, determined by measuring the radiation pattern over a 3D sphere for radiated power calculation, and $|S_{21}|$ is the measured transmission coefficient from PNA port 1 ($P_{\text{tx,pna}}$, the reference plane A) to port 2 ($P_{\text{rx,pna}}$, the reference plane D). Hence, the PA transducer gain, together with the antenna radiation efficiency, is obtained by

$$G_{\text{PA}} \eta_{\text{rad}} = |S_{21}|^2 / (G_{\text{path}} D_{\text{ant}}). \tag{3.8}$$

The PAIAA DC power consumption and the radiated power in the reference plane E is required to calculate the power efficiency in (3.4). P_{DC} is obtained from monitoring the DC power consumption. P_{out} is calculated from $G_{\text{PA}} \eta_{\text{rad}} = P_{\text{out}} / P_{\text{acc}}$, where $G_{\text{PA}} \eta_{\text{rad}}$ is acquired in the measurement (3.8), and P_{acc} is obtained in the additional power calibration.

The product of the PA transducer gain and antenna radiation efficiency is plotted in Fig. 3.7a, in which an average value of 8 dB is observed from 19.5 GHz to 20 GHz. The gain is around 9 dB at 20 GHz, showing a good agreement with the numerical result, although the PA went into compression earlier than expected. The simulation result confirms that the PA goes into compression before reaching the saturated output power as the load impedance differs from the optimal loading condition.

The measured power efficiency is presented in Fig. 3.7b along with the measurement uncertainty of ± 1.5 dB. The uncertainties are mainly caused by the non-ideal measurement environ-

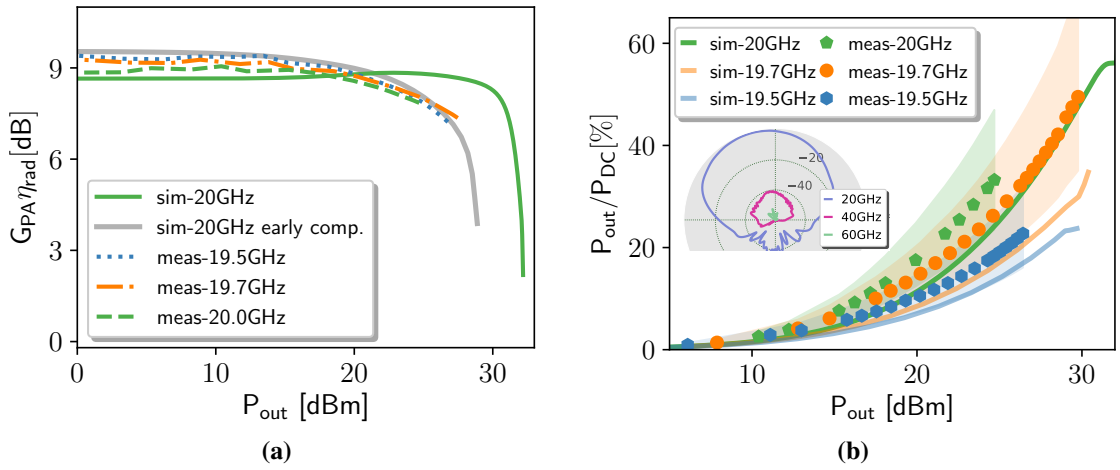


Figure 3.7: (a) The PA transducer gain including the antenna radiation efficiency at reference plane E (see Fig. 3.6b), and (b) the efficiency and measurement uncertainty (±1.5 dB, colored shadows) at the fundamental frequencies versus output power.

ment and setup, such as probe misalignment, reflection from the chamber floor and walls, and tolerance of the reference antenna gain and the power equipment. Note that the frequency shift in the measurement results is assumed to be caused by manufacturing and assembly tolerances. For instance, the permittivity variation in PCB laminates, CNC milling tolerance of the slot cavity periphery, and the impedance mismatch introduced in microwave connector assembly and wire bonding. The simulated radiation patterns of the second and third harmonics are shown in the inset of Fig. 3.7b, where the level of harmonic radiation is at least 40 dB lower than of the fundamental. A maximum active antenna gain of 15 dBi and a peak power efficiency of 50% have been demonstrated in the PAIAA design. The measured radiation patterns are shown in Fig. 3.8, which are in good agreement with the simulated results. A comparison with the state-of-the-art PAIAA designs is summarized in Table 3.3.

The comparison reveals that the power efficiency and the equivalent isotropically radiated power (EIRP) of the PAIAA design are comparable to the C-band design [44], yet with a considerably smaller electrical size and at much higher operating frequencies. The proposed design has demonstrated that a PAIAA element with high peak efficiency (49.5% at 19.7 GHz) and output power (28 dBm) can be achieved by the direct integration method in conjunction with the proposed PA-antenna co-optimization methodology. It is expected to alleviate the thermal dissipation problem by employing a metallic radiating structure of high thermal conductivity, which can be seen as a heat sink. Furthermore, the proposed PAIAA is compact ($0.6\,\lambda \times 0.5\,\lambda$) and applicable to active beamforming antenna arrays.

The main possible areas of improvement for the PAIAA element are:

a) to increase the relative frequency bandwidth from currently 1.5% to at least 10% and move from 20 to 30 GHz;

b) to realize custom PA MMIC designs to minimize PAIAA form factor and increase the

Table 3.3: Performance comparison of the state-of-the-art PAIAAs.

	No OIMN*	Thermal handling	Transistor Technology	Center Frequency	$P_{1dB,out}$	EIRP	PAE peak	Dimensions $L \times W \times H$ [λ^3]
[41]	✓	poor	*p*HEMT	2 GHz	21.7 dBm	N/A	>60%	$0.6 \times 0.8 \times$ N/A
[43]		poor	GaAs	4.15 GHz	28.2 dBm	N/A	60.9%	N/A
[44]		great†	GaN HEMT	5.8 GHz	38 dBm	44.6 dBm	59.93%	$1.9 \times 1.9 \times 2.1$
[42]	✓	poor	AlGaN/GaN	7.25 GHz	30.3 dBm	N/A	42%	N/A
[46]	✓	poor	SiGe HBT	24 GHz	5.6 dBm	4.6 dBm	N/A	$0.2 \times 0.1 \times$ N/A
[57]	✓	poor	0.18 µm CMOS	24 GHz	N/A	N/A	25.6%	$0.3 \times 0.2 \times$ N/A
[47]		poor	GaAs *p*HEMT	35 GHz	N/A	N/A	N/A	$0.8 \times 0.8 \times$ N/A
[58]		poor	BiCMOS	60 GHz	12.8 dBm	9.5 dBm	N/A	$0.2 \times 0.2 \times$ N/A
[45]	✓	poor	BiCMOS	79 GHz	19 dBm	3 dBm	11%‡	$0.4 \times 0.4 \times$ N/A
[B]	✓	good	GaN HEMT	20 GHz	24.7 dBm	30.7 dBm	34.8%	$0.6 \times 0.5 \times 0.3$

*output impedance matching network †installed on a Peltier unit ‡simulated results

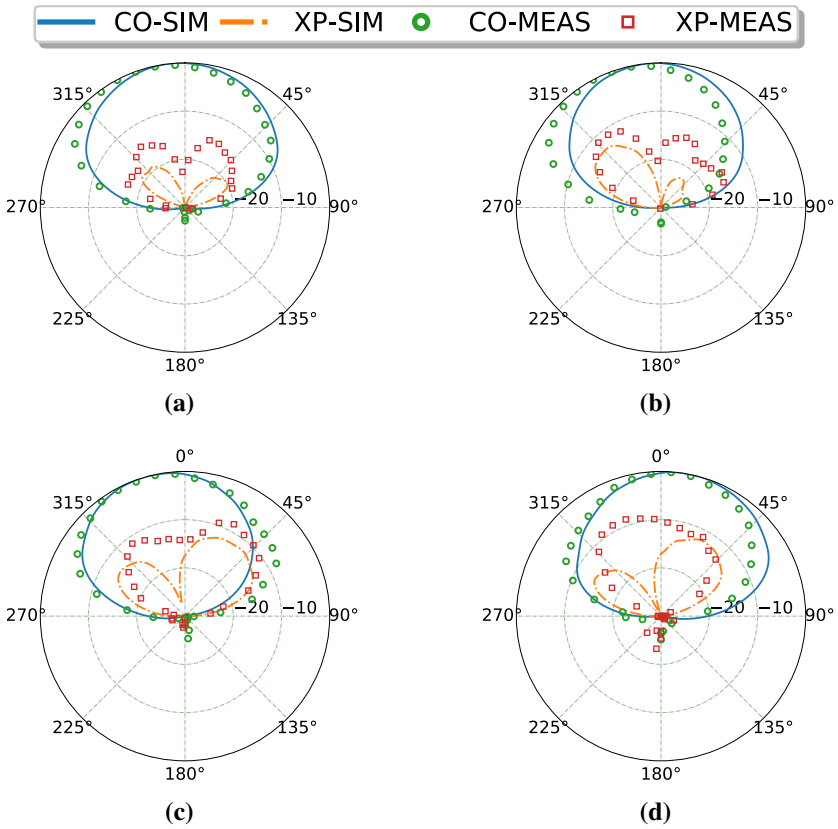


Figure 3.8: Normalized radiation pattern cuts of the PAIAA element (Fig. 3.4) at 19 GHz on (a) $\phi = 0°$ and (b) $\phi = 90°$, and at 20 GHz on (c) $\phi = 0°$ and (d) $\phi = 90°$.

integration level, in particular, to allow for a custom impedance interface between the radiating element and the PA;

c) to scale up the design to arrays of new AIA elements with a higher center frequency at 28 GHz.

The improved AIA design should be done while maintaining the AIA element size at around $0.5\,\lambda \times 0.5\,\lambda$. An active integrated array antenna element with improved system performance is presented in Chapter 6.

CHAPTER 4

ANALYSIS OF SMALL-SCALE ACTIVE INTEGRATED ANTENNA ARRAYS

Antenna mutual coupling effects in active integrated antenna arrays are investigated through the scattering parameters re-normalization technique that extends the application of conventional approaches for passive arrays to active integrated array antennas. Furthermore, a study on the PA-antenna interface impedance variation illustrates various system-level design trade-offs involving PAE, output power, and PA linearity.

4.1 Mutual Coupling in Highly Integrated Active Array

In MU-MIMO (multi-user, multiple-input, multiple-output) scenarios, all PAs transmit different signals to various receivers, resulting in time-variant excitation of the array antenna elements, and thus time-variant loading condition of the PAs. This is different from the single-beam or phase-steered array scenarios. Also, the PA characteristics (e.g., PAE, transducer gain, output power) are affected by antenna element mutual coupling effects and related crosstalk between the transmitter channels [72]. Consequently, accounting for and subsequently understanding the MC effects are essential for active integrated array antenna (AIAA) designs.

Presently, there exist many studies on antenna MC. Craeye et al. conducted a comprehensive review of antenna array MC analysis methods to model these coupling effects [73], which shows that studies are primarily for passive antenna arrays or active antenna arrays assuming a single port model. The MC effects for active receivers were discussed in [74]–[79], in which both analytical and numerical models were proposed and experimentally verified. In those papers, the system receiving sensitivity was affected by the noise at the receiver inputs that partly couples and re-enters the system via the mutually coupled antenna elements.

A combined EM-circuit *multiport* analysis (see Section 3.1) has been proposed to tackle the

design challenges in multiport active integrated antennas by taking account of the interactions of the power waves between those ports. In this respect, arrays of such AIA elements are more complex to characterize in terms of antenna MC effects than conventional arrays, i.e., passive antenna arrays or active antenna arrays with a single port reference impedance per element [73]. This complexity comes from the fact that a common approach of using a standard 50 Ω normalized *S*-matrix for evaluating coupled port powers is no longer representative whenever the ports are terminated with impedances different from 50 Ω. In that case, the *S*-matrix does not directly represent the actual power-wave coupling and reflection coefficients, although these models are mathematically correct.

The following section demonstrates that *S*-matrices must be re-normalized appropriately to represent the exact port termination so that it can provide physical insights into the actual MC of power waves in integrated active transmitting antenna arrays, including the isolation level between the *drain* port (output) and the *gate* port (input) of the transistor. This re-normalization procedure can help improve the overall system performance in terms of port isolation and circuit stability to avoid undesired oscillation in the AIAAs.

Scattering Matrix Re-Normalization

The PAIAA element from the previous chapter was modeled as a multiport circuit. To interpret the MC effects from the *S*-matrix of an array of such elements, it is required to re-normalize the *S*-matrix with proper port reference impedances ($\mathcal{Z}_i' \neq 50\ \Omega$, $i = 1,2,\ldots,N$). To this end, we follow the normalization procedure in [80]. The re-normalized *S*-matrix $\mathcal{S}'$ is generally different from the standard 50-Ω *S*-matrix $\mathcal{S}$ and can be expressed in terms of $\mathcal{S}$ as

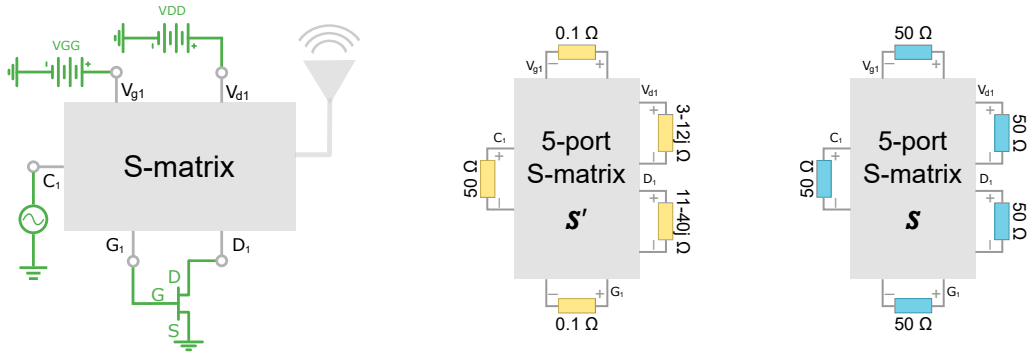
$$\mathcal{S}' = \mathcal{A}^{-1}(\mathcal{S} - \Gamma^{\mathrm{H}})(\mathcal{I} - \Gamma\mathcal{S})^{-1}\mathcal{A}^{\mathrm{H}}\,, \tag{4.1}$$

where H denotes conjugate transpose, and Γ and $\mathcal{A}$ are the diagonal matrices with their i-th diagonal components being r_i and $(1-r_i^*)\sqrt{|1-r_i r_i^*|}/|1-r_i|$, respectively; r_i is the power wave reflection coefficient of $\mathcal{Z}_i'$ with respect to $\mathcal{Z}_i^*$, that is,

$$r_i = \frac{\mathcal{Z}_i' - \mathcal{Z}_i}{\mathcal{Z}_i' + \mathcal{Z}_i^*}.$$

Fig. 4.1a illustrates the PAIAA diagram. The power wave interactions within the circuitry and antenna designs, solved in the EM environment, are expressed by the *S*-matrix (grey block). This diagram corresponds to the *S*-matrix re-normalization concept in Fig. 4.1b, where the *S*-matrix $\mathcal{S}'$ is re-normalized with port reference impedance $\mathcal{Z}_i'$ $(i = 1,2,\ldots,5)$. $\mathcal{Z}_i'$ are chosen in such a way that it represent the actual port terminations (i.e., the output impedances of the interconnected circuits) to provide a more representative physical insight into the power-wave coupling behavior of the PAIAAs. The concept of the standard 50 Ω normalization is shown in Fig. 4.1c for comparison.

The PAIAA model can be described as follows (Fig. 4.1a): Port 1 is connected to the sig-



(a) **(b)** $\mathcal{S}'$ **(c)** $\mathcal{S}$

Figure 4.1: (a) Diagram of the scattering matrix of the five-port PAIAA from combined EM-circuit simulation. Diagram of the scattering matrix of the 5-port PAIAA (b) with reference impedances $\mathcal{Z}_i'$ for an isolated antenna element as shown in Fig. 3.4 and (c) with standard 50 Ω as the port reference impedance.

nal input source (C_1); port 2 and port 3 are connected to the transistor drain (output) and gate (input); port 4 and port 5 are connected to a DC power supply for biasing the drain and gate, respectively. The chosen port reference impedances of port 2 and port 3 need to represent the output and input impedance of the Qorvo TGF2942 GaN HEMT (modeled result from the Modelithics small-signal model is used herein). The biasing ports (port 4 and port 5) have to be (near-)short-circuited (at f_0) while the reference impedance at port 1 remains at 50 Ω. Hence, the ports in the PAIAA have different reference impedances for re-normalization. This outcome is counterintuitive to the standard *S*-matrix normalization, in which $\mathcal{Z}_i'$ is typically assumed to be 50 Ω.

The mutual coupling effects in AIAAs can be divided into two categories:

Intra-element MC MC effects between ports belonging to the same element.

Inter-element MC MC effects between ports belonging to different elements.

The magnitude of the re-normalized *S*-matrix elements (dB($|\mathcal{S}_{ij}'|$)) at the center frequency ($f_0 = 20\,\text{GHz}$) of a five-port single PAIAA element is presented in Fig. 4.2b, in which the diagonal terms represent the reflection coefficient at the corresponding ports. Below are the notations of the "antenna ports":

- C_m – the *coaxial* port of the AIA element,
- D_m – the *drain* port of the transistor,
- G_m – the *gate* port of the transistor,
- V_{dm} – the biasing port at the drain side of the transistor,
- V_{gm} – the biasing port at the gate side of the transistor,

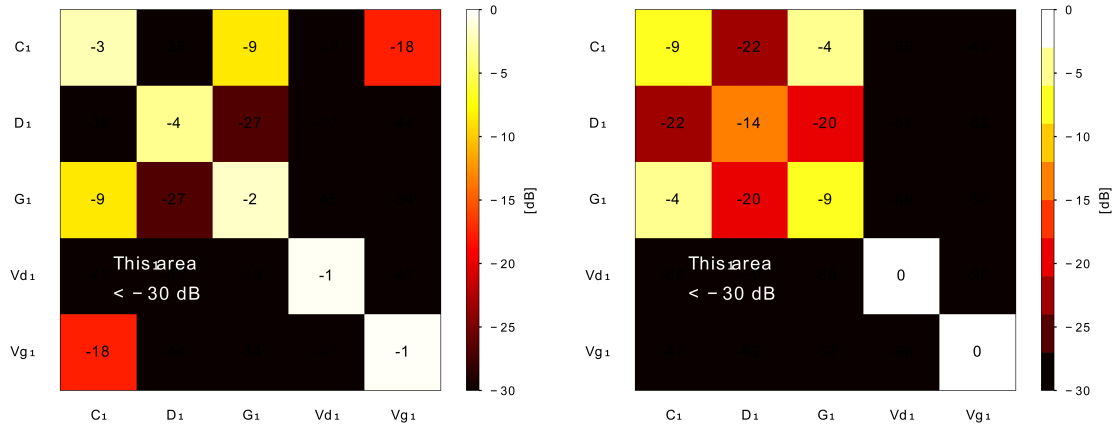


Figure 4.2: Magnitude of the *S*-matrix (a) normalized with 50 Ω (see Fig. 4.1c) and (b) re-normalized with the port reference impedances $\mathcal{Z}_i'$ denoted in Fig. 4.1b of a single PAIAA element as shown in Fig. 3.4.

where m indicates the m-th element in the AIAA. For instance, $(\mathrm{C}_1,\mathrm{C}_1)$ in Fig. 4.2b represents $\mathrm{dB}(|\mathcal{S}'_{\mathrm{C}_1\mathrm{C}_1}|)$; i.e., the reflection coefficient at the input port of the first AIA element, which is -9 dB in this case.

The passive antenna *S*-matrix $\mathcal{S}'_{ij}$ *de facto* describes the inter-port MC effects in the absence of PA amplification. In Fig. 4.2b, $\mathrm{dB}|\mathcal{S}'_{\mathrm{D}_1\mathrm{G}_1}|$ indicates no amplification between port 2 *drain* and port 3 *gate*; this is generally not the case for transistors in amplifier networks. $\mathrm{dB}|\mathcal{S}'_{\mathrm{D}_1\mathrm{G}_1}| = -20$ dB shows that the MC effects between the two ports[1] are relatively weak, suggesting a low level of OTA feedback between the two ports hence a low chance of circuit oscillation. Similarly, $\mathrm{dB}|\mathcal{S}'_{\mathrm{D}_1\mathrm{C}_1}|$ indicates that the OTA coupling level[1] between port 2 *drain* and port 1 *coaxial* is -22 dB; this can be seen as a sufficient level of isolation between the amplifier input and output, provided that the amplifier gain is lower than the feedback by a sufficient margin. Furthermore, the reflection coefficient at port 2 *drain* $\mathrm{dB}|\mathcal{S}'_{\mathrm{D}_1\mathrm{D}_1}|$ is not significantly low. This is not due to poor impedance matching at the port but because the antenna impedance is not conjugately matched to the output impedance of the PA. As mentioned in [81], the interface impedance was chosen to maximize the PAE based on the load-pull result, of which the large-signal optimal loading condition is generally different from the conjugate match of the small-signal analysis. $\mathrm{dB}|\mathcal{S}'_{\mathrm{D}1_1\mathrm{D}_1}| = -14$ dB suggests that a decent power gain can be obtained because a conjugate matching condition at the PA output is required to maximize the power gain. As mentioned before, the two biasing ports $\mathrm{V}_{\mathrm{d}m}$ and $\mathrm{V}_{\mathrm{g}m}$ should represent (near-)short circuits, which explains the (near-)complete reflections at these ports.

This re-normalization technique can also be applied to multiport PAIAA arrays. We can exemplify this application for a linear array of two elements, as shown in Fig. 4.3. The 50 Ω normalized *S*-matrix in Fig. 4.4a is now a 10×10 matrix (five ports per element). The 10×10

[1] in the absence of transistor amplification

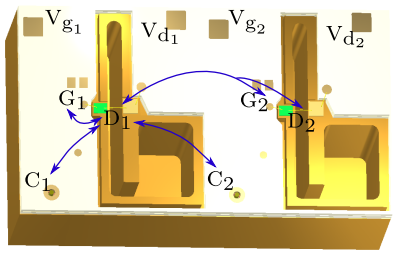


Figure 4.3: An illustration of mutual coupling effects between the ports in the multiport two-element PAIAA array.

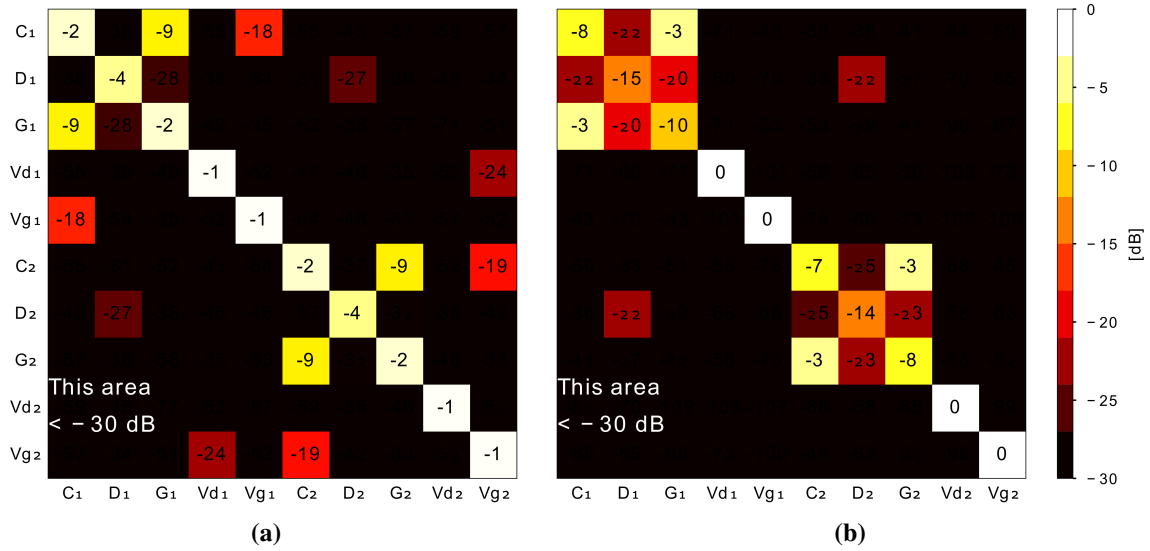


Figure 4.4: Magnitude of the *S*-matrix (a) normalized with 50 Ω and (b) re-normalized with the port reference impedances $\mathcal{Z}_i'$ denoted in Fig. 4.1b of the linear PAIAA array shown in Figure 4.3.

S-matrix is subsequently re-normalized with the port reference impedances $\mathcal{Z}_i'$ by using (4.1), as shown in Fig. 4.4b. In the array scenario, the MC effects not only exist between the ports in the same element (*intra-element MC*), but can also occur between the ports located in different elements (*inter-element MC*). For instance, $\mathrm{dB}|\mathcal{S}'_{\mathrm{D_2D_1}}| = -22\,\mathrm{dB}$ is the isolation level between the drain port of the first element $\mathrm{D_1}$ and of the second element $\mathrm{D_2}$. Those two ports have the most substantial inter-element MC effects as they are used to excite the radiators.

Conclusion

The standard 50 Ω normalized *S*-matrix commonly applied in antenna MC parameters analysis is not fully representative in quantifying the intra-element nor inter-element MC effects of power waves in highly integrated transmitting antenna arrays. This section proposes an *S*-matrix re-normalization procedure that assumes the port reference impedances equal to the actual port terminations or the output impedance of the driving sources. This technique provides an insight-

ful physical interpretation of the mutual coupling coefficients of power waves in integrated array antennas, of which the analysis is performed assuming the absence of transistor amplification (i.e., we set $S_{21}^{\mathrm{PA}} = S_{12}^{\mathrm{PA}} = 0$).

When applying the re-normalization technique to characterize an array of two AIA elements, the following critical observations can be made:

- The intra-element OTA coupling level between the drain port and the corresponding gate port is $\mathrm{dB}|\mathcal{S}'_{\mathrm{G}_i\mathrm{D}_i}| \leq -20\,\mathrm{dB}$. The isolation level between the amplifier output and input is an essential performance metric in PA designs when it comes to, for example, circuit stability.
- The inter-element OTA coupling level from the drain port of the first element to the drain port of the second element is the strongest, which is expected because these ports are employed to excite the radiating slots.
- The reflection coefficient at the drain port is not significantly low; this is not due to a poor antenna impedance match to the PA output, as could be concluded at first glance. In fact, the interface impedance was chosen for the maximum PAE, which is typically different from a conjugate match at the PA output. Yet, $\mathrm{dB}|\mathcal{S}'_{\mathrm{D1}_1\mathrm{D}_1}| = -14\,\mathrm{dB}$ indicates that a decent power gain can be attained since a conjugate match is needed for a high power gain.

4.2 Amplifier Load Matching Effects and Design Trade-Off Examples

Power efficiency and linearity are among the key performance metrics in 5G and beyond wireless communication systems. To avoid additional complex linearization techniques, this section focuses on studying PAIAAs based on class AB amplifiers for a trade-off between high energy efficiency and linearity.

Recently, various PA architectures and their susceptibility to load mismatch were studied in [82]. It concluded that some PA architectures are more susceptible to load mismatch that can lead to significant degradation of linearity and are, therefore, not applicable to active antenna systems exhibiting strong mutual coupling effects (see Section 4.1). The importance of PA loading conditions and their impact on system performance, such as linearity and power efficiency, are investigated in the present section. To demonstrate the eminence of optimal PA loading conditions in AIAs, the PAIAA design example in Section 3.2 is used as a starting point. The antenna impedance of the PAIAA is tuned to meet various prioritized design parameters while the PA design remains unchanged.

All design examples presented in this section are based on two-tone testing of a co-simulated model in ADS and Ansys HFSS [83] at the fundamental frequency $f_0 = 20\,\mathrm{GHz}$, where the drain voltage $V_{\mathrm{ds}} = 20\,\mathrm{V}$ and the drain current $I_{\mathrm{dq}} = 52\,\mathrm{mA}$ are set for the GaN HEMT model. Three specific design examples for the isolated antenna element have been considered, which have been optimized to achieve the maximum PAE (Example 1), maximum linearity (Example 2), and a trade-off between both (Example 3). Conjugate matching is a common practice to attain a maximum power transfer in passive circuits. Nevertheless, the maximum voltage of the

transistor is bounded by the breakdown voltage, and the maximum current swing is determined by the device size [37], [39]. Hence, the optimal load impedance of PAs is generally different from the conjugate of the PA output impedance. The conjugately matched PA-antenna design is shown in the design examples as the baseline. Lastly, an array antenna design case focuses on antenna MC effects and crosstalk between PAs during beam steering.

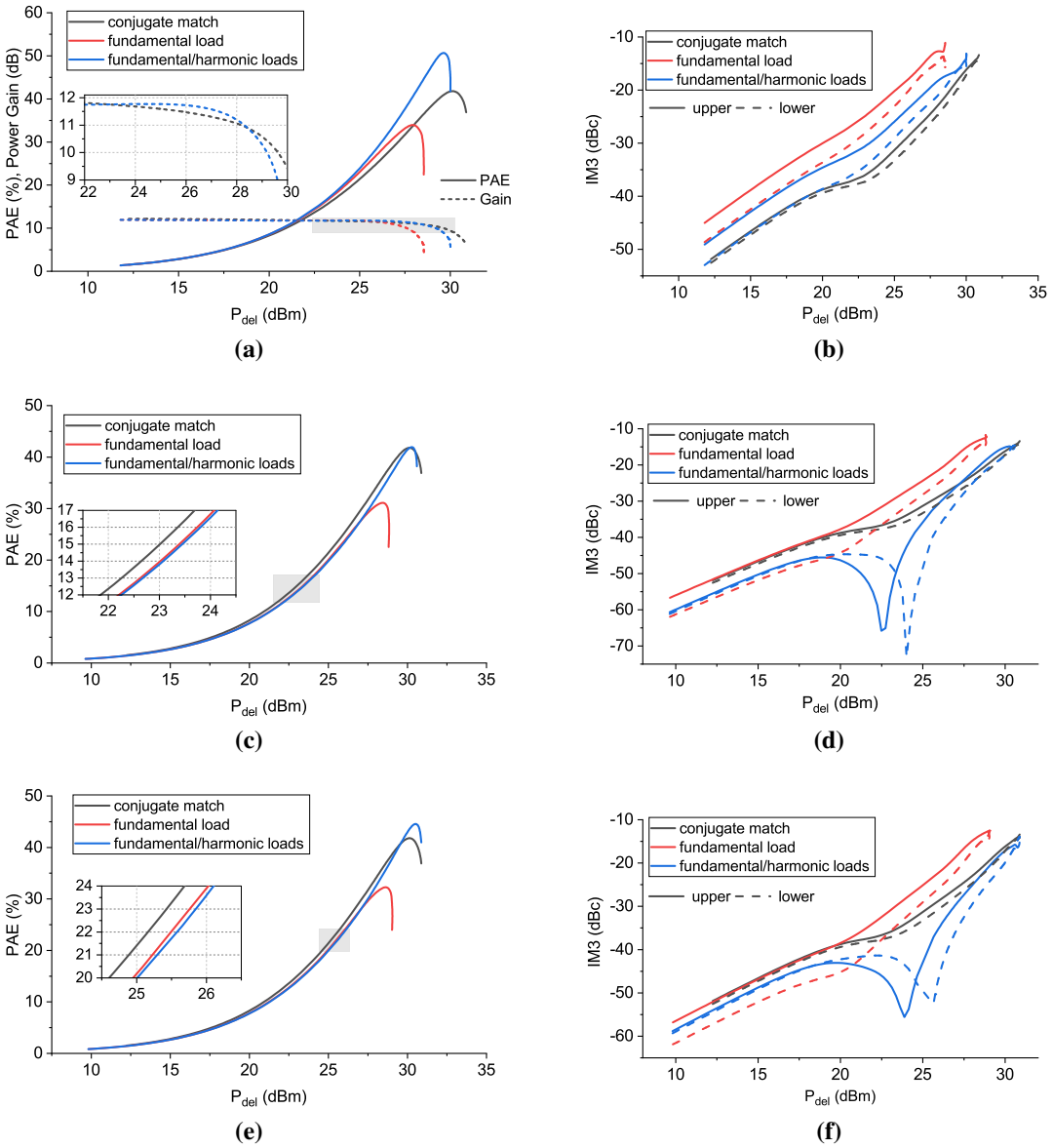


Figure 4.5: Simulated PAE and IM3 (upper IM3-solid, lower IM3-dashed) for (a)(b) the maximum PAE (design example 1), (c)(d) the maximum linearity (design example 2), and (e)(f) a trade-off of PAE and linearity (design example 3), respectively. The conjugately matched design is plotted (black) for comparison.

Design Example 1—Optimum PA Loading for Maximum PAE

A single PAIAA element is designed for maximized PAE at the 1 dB compression point[1] (P1dB = 28.3 dBm). The optimal PA load impedances for this case are found through load pull analysis and are equal to $Z_{\text{opt},f_0} = 7 + j39\ \Omega$, $Z_{\text{opt},2f_0} = 1 + j25\ \Omega$, and $Z_{\text{opt},3f_0} = 1 + j12\ \Omega$. These optimal load impedance values at the fundamental and harmonic frequencies are then synthesized in the antenna design.

For comparison, the design example based on the traditional conjugate impedance match at the PA output ($Z_{\text{cm},f_0} = 18 + j42\ \Omega$) of the small-signal model is also considered. Fig. 4.5a shows that a 10% improvement in PAE at P2dB[2] ($P_{\text{del}} = 29.2$ dBm) can be obtained by simultaneously matching the optimal fundamental and harmonic loads. The power gain realized for the conjugately matched design shows an earlier gain compression than the optimized design, suggesting a lower P1dB level.

Design Example 2—Maximum Linearity

In mobile applications, such as long term evolution (LTE) and microwave backhaul, a peak to average power ration (PAPR) of several decibels (e.g., 3–10 dB) represents normal operating conditional [60]. Accordingly, the optimization of the IM3[3] at 6 dB BO is considered in this case, where PAE is not of top priority. The 6 dB BO is $P_{\text{del}} = 23.3$ dBm in this example, where the designed antenna impedances satisfying the optimization loading condition are $Z_{\text{opt},f_0} = 7 + j34\ \Omega$, $Z_{\text{opt},2f_0} = 1 + j25\ \Omega$, and $Z_{\text{opt},3f_0} = 2 + j20\ \Omega$. The antenna design synthesizing the required optimal loading conditions shows a significant improvement of 16 dB in IM3 at 6 dB BO, as shown in Fig. 4.5d.

Design Example 3—A trade-off between PAE and Linearity

This design seeks a trade-off between PAE and linearity at 3 dB output BO, $P_{\text{del}} = 25.5$ dBm, by enhancing the IM3 without compromising the PAE. The loading condition of this "balanced" optimization is $Z_{\text{opt},f_0} = 7 + j34\ \Omega$, $Z_{\text{opt},2f_0} = 1 + j24\ \Omega$, and $Z_{\text{opt},3f_0} = 1 + j12\ \Omega$. In two-tone testing, the IM3 with these antenna impedances at the fundamental and harmonic frequencies in the lower band has demonstrated an evident improvement of 21 dB at 3 dB BO as seen in Fig. 4.5f, while the PAE, shown in Fig. 4.5e, drops by merely 1%, as compared to the conjugate match design.

Discussion—Isolated Element Designs

Fig. 4.6 compares the PAE and linearity of three isolated PAIAA element designs, and the comparison is summarized in Table 4.1. This cross-comparison provides a distinct insight into how

[1] P1dB: The output power level where the gain decreases by 1 dB from its low-power value.
[2] The 2 dB compression point, i.e., where the gain has decreased by 2 dB from its lower-power value.
[3] The third-order intermodulation power level relative to the fundamental tones (dBc).

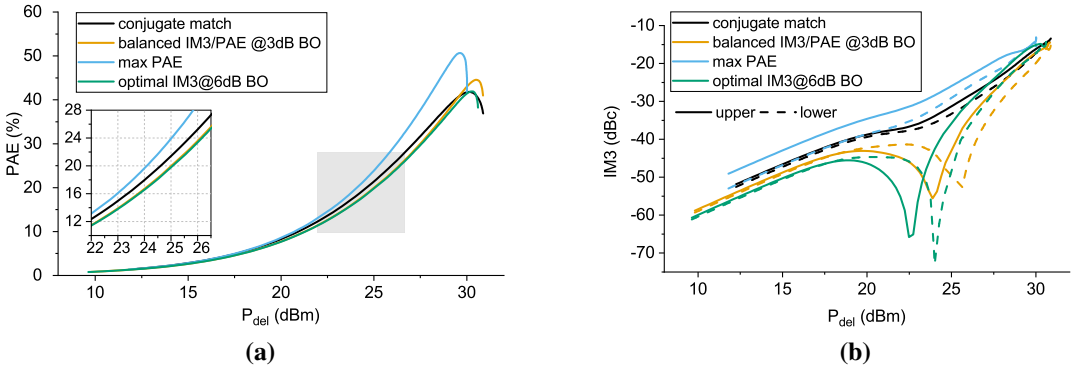


Figure 4.6: Comparison of presented design cases with various weighted performance metrics: (a) PAE, (b) upper IM3 (solid line), and lower IM3 (dashed line) of the PAIAA design with the loading condition of conjugate match, balanced IM3 and PAE, maximum PAE, and optimal linearity.

the interface impedance can be leveraged in PAIAA elements with different design trade-offs. Therefore, the PA-antenna jointly optimized design methodology (Section 3.1) is required in AIA designs to optimize the prioritized design parameters and avoid design "weaknesses".

Five-Element Linear Array Antenna

Design examples of a five-element PAIAA linear array (Fig. 4.7a) with improved linearity are considered. The goal is to minimize the IM3 of the array by synthesizing the optimal loading

Table 4.1: Performance trade-offs for design examples of different prioritization criteria.

		Prioritization Criteria			
		Maximum PAE @P1dB	Optimal IM3 @6 dB BO	Balanced IM3/PAE @3 dB BO	Conjugate Match
6 dB BO	PAE	17.2%	14.5%	14.9%	15.8%
	$IM3_{upper}$	−29.9 dBc	−51.5 dBc	−50.7 dBc	−35.4 dBc
	$IM3_{lower}$	−33.5 dBc	−48.9 dBc	−42.2 dBc	−36.8 dBc
3 dB BO	PAE	26.6%	21.7%	22.3%	23.5%
	$IM3_{upper}$	−24.0 dBc	−32.7 dBc	−37.1 dBc	−29.8 dBc
	$IM3_{lower}$	−36.9 dBc	−40.3 dBc	−52.6 dBc	−31.8 dBc
P2dB	PAE	49.3%	38.0%	38.9%	39.5%
	$IM3_{upper}$	−16.5 dBc	−17.1 dBc	−19.9 dBc	−18.7 dBc
	$IM3_{lower}$	−16.7 dBc	−20.0 dBc	−23.5 dBc	−20.4 dBc

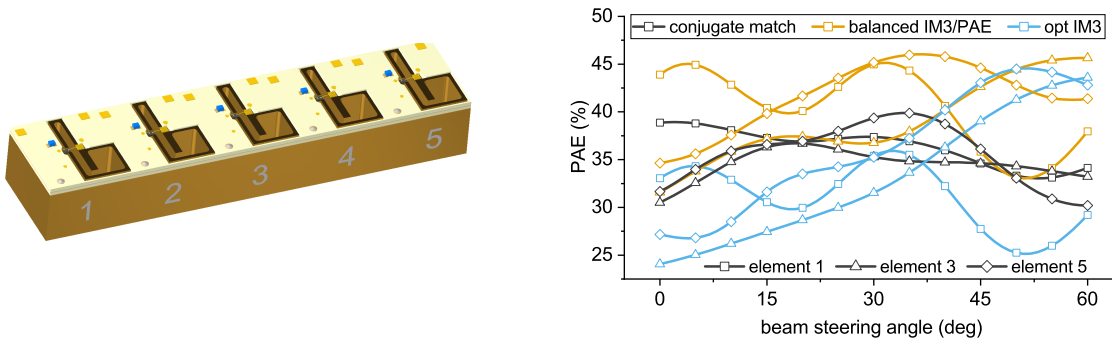


Figure 4.7: (a)Illustration of the linear 5-element PAIAA array (b) PAE of antenna elements in the PAIAA array of conjugate match, balanced trade-off of IM3 and PAE loading, and optimal linearity loading.

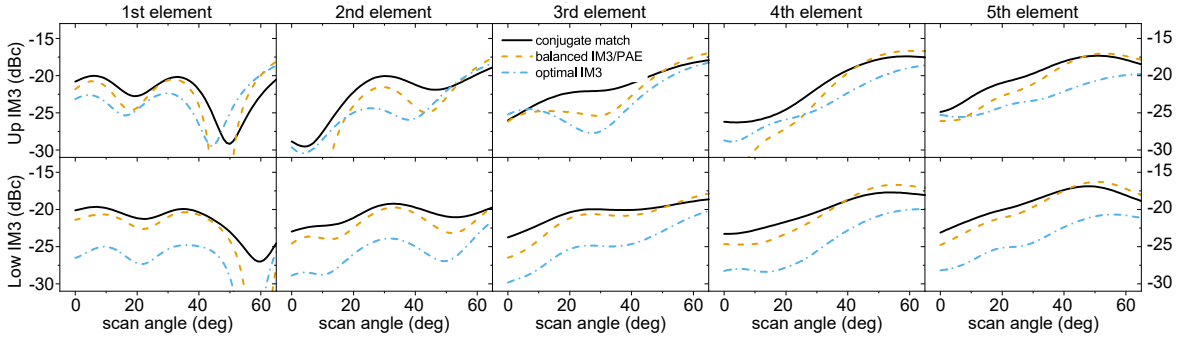


Figure 4.8: Upper and lower IM3 of the 5-element PAIAA array with designed antenna impedance of conjugate match (solid black line), trade-off of linearity and PAE (dashed yellow line), and optimal linearity (dash-dotted blue line) while scanning. The elements are driven by $P_{avs} = 20\,\text{dBm}$ ($P1dB_{in} = 23.5\,\text{dBm}$).

condition at the fundamental frequency and harmonic frequencies with the antenna design. In the design examples, a single element is optimized for (*i*) the best linearity and (*ii*) the best trade-off between linearity and efficiency. The array of five such elements has been examined with these loading conditions. Moreover, optimizing the PAIAA array element-by-element can further improve the linearity, power, or PAE if needed. The IM3 of the balanced IM3/PAE array is improved by a few decibels (Fig. 4.8), and the PAE is overall higher than the conjugately matched array (Fig. 4.7b). The IM3 in the lower frequency band of the array of the optimal-IM3 elements is 6 dB lower than the conjugately matched array (Fig. 4.8). As mentioned before, when linearity becomes the sole design parameter, the PAE of the PAIAA elements degrades from optimizing the linearity (Fig. 4.7b). This outcome might be acceptable in particular communication systems; however, if the power efficiency is also a vital system performance metric, one needs to be more attentive to the design trade-offs between the design parameters.

4.3 Conclusion

The standard 50 Ω normalized *S*-matrix, commonly employed in studying the mutual coupling effects in passive arrays, no longer applies to interpreting the coupling effects in highly integrated multiport active array antennas. Re-normalizing the *S*-matrix with impedances representing the actual port terminations or the output impedance of the driving sources allows for a physical interpretation of the mutual coupling effects in integrated multiport active array antennas. Such a re-normalized *S*-matrix provides insight into the ports isolation level in integrated active array designs and may help to identify possible system oscillation.

Additionally, design examples of optimal PA load matching for different performance metrics (e.g., output power, PAE, power gain) are presented in this chapter. Those examples show that the design parameters of the PA integrated antenna elements and an array of such elements can be optimized through direct integration and custom antenna designs at the fundamental and higher harmonic frequencies. Consequently, the optimal design trade-off of the PAIAAs can be made at the system level instead of at the component level.

CHAPTER 5

ACTIVE INTEGRATED UNIT CELL AND INFINITE ARRAY WAVEGUIDE SIMULATOR

This chapter presents a cost-effective approach for verifying active integrated antenna elements in an infinite array environment. The definition of an active integrated unit cell of infinite active arrays is introduced. The infinite array waveguide simulator technique, a widely known design approach for beamsteering passive arrays, is extended to active integrated arrays.

5.1 Active Integrated Unit Cell

This section focuses on the design example of an active integrated unit cell (AIUC) of infinite array antennas, which can also be treated as the antenna element design for large-scale active arrays. A performance metric that accounts for the electromagnetic coupling effects and the PA's nonlinear behavior in the AIUC, the *active scan element pattern*, is proposed.

An AIUC is developed for a rectangular planar array at the center frequency $f_0 = 20\,\text{GHz}$ based on the design example in Sec. 3.2. The design has been modified from the initial PAIAA design such that the co-polarized field component is parallel to the planes of symmetry, which is required for applying the infinite array waveguide (WG) simulator technique [84]. Fig. 5.1 depicts the AIUC design, comprising a metallic radiating structure and a Rogers RO4350B multilayer PCB. Two slots symmetric with respect to the *xz*-plane are introduced as the design parameters of the antenna impedance, and a ridge is added in the larger slot to increase the equivalent electrical length without increasing the physical size. The radiation characteristics, such as the radiation resistance and radiation pattern, are mainly determined by the *x*-directed slot, while the *y*-directed slots primarily affect the reactance. The same GaN HEMT from the previous design is employed. The direct integration technique is applied herein to improve the power efficiency and reduce the form factor of the AIA element.

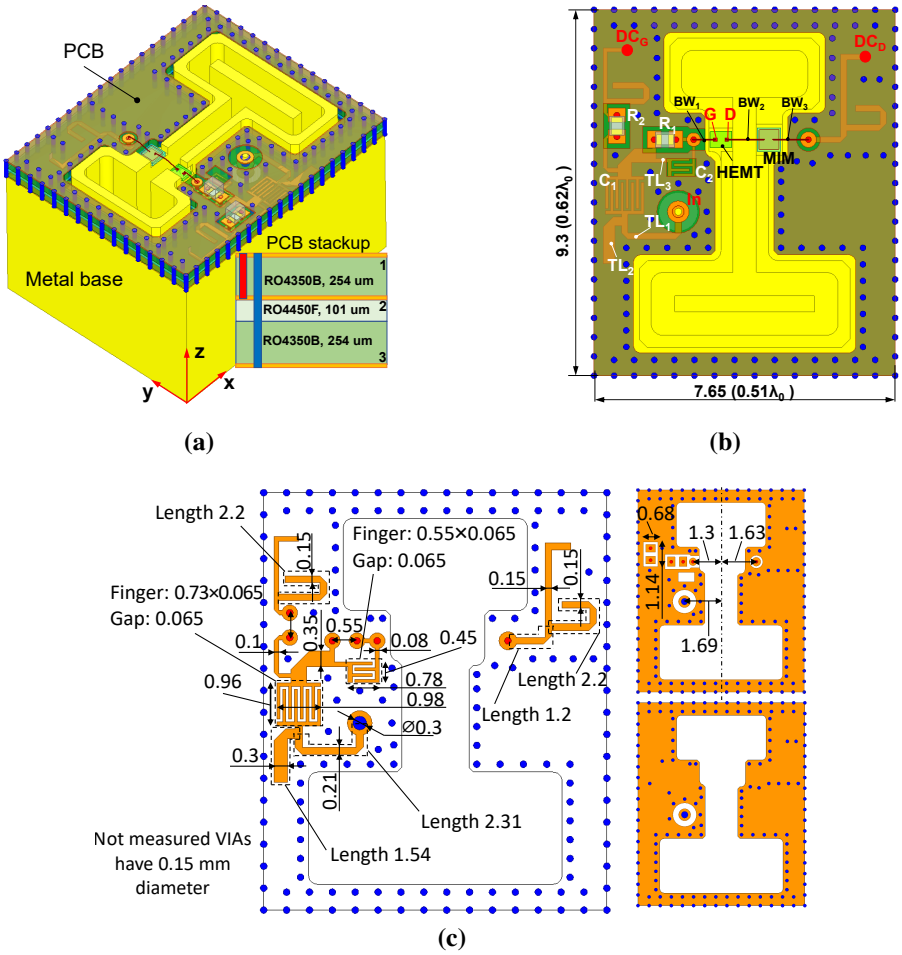


Figure 5.1: The AIUC design: (a) 3D view (inset: the PCB stackup), (b) top view, (c) and the PCB layout with primary design dimensions: enlarged inner layer (*left*), top layer (*top right*), bottom layer (*bottom right*). Through VIAs (blue) connect all layers; blind VIAs (red) connect the top layer and inner layer (unit: mm).

Active Scan Element Pattern

The conventional scan element pattern (SEP) applies the EM field superposition principle [85], [86] and the reciprocity theorem [87]. Nevertheless, neither of these principles applies to AIUCs due to the nonlinear and nonreciprocal nature of PAs, where the former leads to a dependence on the AIUC input power. The AIUCs' radiating property is herein characterized by employing the below-defined equivalent power-dependent *active scan element pattern* (ASEP) to account for PAs' nonlinear nature.

The electric and magnetic field components $(\mathscr{E}, \mathscr{H})$ of a propagating wave in the direction of the z-axis in an infinite AIAA environment can be represented in terms of the Floquet modal

functions as

$$\mathscr{E} = \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} \mathcal{A}_{mn}^{\mathrm{TE}} \boldsymbol{e}_{mn}^{\mathrm{TE}} \exp\{-k_{zmn}z\} + \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} \mathcal{A}_{mn}^{\mathrm{TM}} \boldsymbol{e}_{mn}^{\mathrm{TM}} \exp\{-k_{zmn}z\} \tag{5.1}$$

$$\mathscr{H} = \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} \mathcal{A}_{mn}^{\mathrm{TE}} \boldsymbol{h}_{mn}^{\mathrm{TE}} \exp\{-k_{zmn}z\} + \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} \mathcal{A}_{mn}^{\mathrm{TM}} \boldsymbol{h}_{mn}^{\mathrm{TM}} \exp\{-k_{zmn}z\} \tag{5.2}$$

where $\boldsymbol{e}_{mn}^{\mathrm{TE/TM}}$ and $\boldsymbol{h}_{mn}^{\mathrm{TE/TM}}$ are the electric and magnetic vector modal functions of the TE_{mn} (transverse electric to z) and TM_{mn} (transverse magnetic to z) Floquet modes [86]. TE_{mn} and TM_{mn} Floquet vector modal functions are sets of orthogonal functions that are normalized with respect to the modal power $P_{mn}^{\mathrm{TE/TM}}$ and utilized to express the EM fields of an infinite array. $\mathcal{A}_{mn}^{\mathrm{TE/TM}}$ are the constant modal amplitudes dependent on the desired radiation direction (θ_s, ϕ_s) and input available power P_{avs}. The electric vector modal functions are represented in the normalized forms [86]

$$\boldsymbol{e}_{mn}^{\mathrm{TE}}(x,y) = \frac{\hat{x}k_{yn} - \hat{y}k_{xm}}{\sqrt{d_x d_y (k_{xm}^2 + k_{yn}^2)\mathcal{Y}_{mn}^{\mathrm{TE}}}} \exp\{-jk_{xm}x - jk_{yn}y\} \tag{5.3}$$

$$\boldsymbol{e}_{mn}^{\mathrm{TM}}(x,y) = \frac{\hat{x}k_{xm} + \hat{y}k_{yn}}{\sqrt{d_x d_y (k_{xm}^2 + k_{yn}^2)\mathcal{Y}_{mn}^{\mathrm{TM}}}} \exp\{-jk_{xm}x - jk_{yn}y\} \tag{5.4}$$

$$\mathcal{Y}_{mn}^{\mathrm{TE}} = \frac{k_{zmn}}{\omega\mu}, \quad \mathcal{Y}_{mn}^{\mathrm{TM}} = \frac{\omega\varepsilon}{k_{zmn}} \tag{5.5}$$

$$k_{xm} = k_{x0} + \frac{2m\pi}{d_x}, \quad k_{yn} = k_{y0} + \frac{2n\pi}{d_y} \tag{5.6}$$

$$k_{x0} = k_0 \sin\theta_s \cos\phi_s, \quad k_{y0} = k_0 \sin\theta_s \sin\phi_s \tag{5.7}$$

where k_0 is the wavenumber in free space, ω is the angular frequency, and ε, μ are the permittivity and permeability of the medium. The longitudinal wavenumber is obtained as $k_{zmn} = \sqrt{k^2 - k_{xm}^2 - k_{yn}^2}$ where k is the wavenumber in the medium. The magnetic field vector modal functions can be found by $\boldsymbol{h}_{mn}^{\mathrm{TE/TM}} = \mathcal{Y}_{mn}^{\mathrm{TE/TM}} \hat{z} \times \boldsymbol{e}_{mn}^{\mathrm{TE/TM}}$. For the chosen modal normalization (5.3), (5.4) $|\mathcal{A}_{mn}^{\mathrm{TE/TM}}|^2/2 = P_{mn}^{\mathrm{TE/TM}}$ for this AIUC design example, where $P_{mn}^{\mathrm{TE/TM}}$ is the power passing through the unit cell. The far field of the infinite array still represents the superposition of the propagating Floquet modes in (5.1) and (5.2). The equivalent electric and magnetic surface currents are expressed by $\boldsymbol{J}_{mn}^{\mathrm{TE/TM}} = \hat{z} \times \boldsymbol{h}_{mn}^{\mathrm{TE/TM}}$ and $\boldsymbol{M}_{mn}^{\mathrm{TE/TM}} = -\hat{z} \times \boldsymbol{e}_{mn}^{\mathrm{TE/TM}}$, where $\hat{z}$ is the unit vector in the direction of the z-axis. The far-field representation can be obtained by the radiation integrals [88]

$$\boldsymbol{e}_{\mathrm{FF}mn}^{\mathrm{TE/TM}}(\boldsymbol{r}) = \mathcal{A}_{mn}^{\mathrm{TE/TM}} \mathcal{C}_{mn}^{\mathrm{TE/TM}} \frac{\exp\{-jkr\}}{4\pi r} \mathcal{I}_{mn}(\theta,\phi), \tag{5.8}$$

where $\boldsymbol{r}$ indicates the observation point (r,θ,ϕ), r is the distance between the observation point

and the source point, and the coefficients $\mathcal{C}_{mn}^{\mathrm{TE/TM}}$ are defined as

$$\mathcal{C}_{\theta mn}^{\mathrm{TE}}(\theta,\phi) = -j\frac{k_{zmn}\cos\theta + k}{\sqrt{\mathcal{Y}_{mn}^{\mathrm{TE}} d_x d_y (k_{xm}^2 + k_{yn}^2)}} \cdot \Big(\sin\phi k_{xm} - \cos\phi k_{yn}\Big) \tag{5.9}$$

$$\mathcal{C}_{\phi mn}^{\mathrm{TE}}(\theta,\phi) = -j\frac{k_{zmn} + k\cos\theta}{\sqrt{\mathcal{Y}_{mn}^{\mathrm{TE}} d_x d_y (k_{xm}^2 + k_{yn}^2)}} \cdot \Big(\cos\phi k_{xm} + \sin\phi k_{yn}\Big) \tag{5.10}$$

$$\mathcal{C}_{\theta mn}^{\mathrm{TM}}(\theta,\phi) = j\sqrt{\mathcal{Y}_{mn}^{\mathrm{TM}}}\frac{k_{zmn} + k\cos\theta}{\sqrt{d_x d_y (k_{xm}^2 + k_{yn}^2)}} \cdot \Big(\cos\phi k_{xm} + \sin\phi k_{yn}\Big) \tag{5.11}$$

$$\mathcal{C}_{\phi mn}^{\mathrm{TM}}(\theta,\phi) = -j\sqrt{\mathcal{Y}_{mn}^{\mathrm{TM}}}\frac{k_{zmn}\cos\theta + k}{\sqrt{d_x d_y (k_{xm}^2 + k_{yn}^2)}} \cdot \Big(\sin\phi k_{xm} - \cos\phi k_{yn}\Big) \tag{5.12}$$

The $\mathcal{I}_{mn}$ term is written as

$$\begin{aligned}\mathcal{I}_{mn}(\theta,\phi) =& d_x d_y \operatorname{sinc}\big((k_x - k_{xm})\frac{d_x}{2}\big)\operatorname{sinc}\big((k_y - k_{yn})\frac{d_y}{2}\big) \\ &\cdot \sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty} \exp\{j(k_x - k_{x0})md_x + j(k_y - k_{y0})nd_y\},\end{aligned} \tag{5.13}$$

where $k_x = k\sin\theta\cos\phi, \quad k_y = k\sin\theta\sin\phi$, and $d_x d_y$ is the AIUC aperture area. The double summation in (5.13) is the array factor (AF) at the beamsteering direction (θ_s, ϕ_s), which can be obtained by [86]

$$\mathrm{AF}(\theta,\phi) = \frac{4\pi^2}{d_x d_y}\sum_{m=-\infty}^{\infty}\sum_{n=-\infty}^{\infty}\delta(k_x - k_{xm})\delta(k_y - k_{yn}). \tag{5.14}$$

The Dirac delta functions in (5.14) indicate that the AIAA radiates only at discrete angles, which was expected from (5.1), (5.2). During beamsteering, the direction of interest is (θ_s, ϕ_s), i.e., $k_x = k_{x0}, k_y = k_{y0}$. Substituting this into (5.8), one can observe that only $\mathcal{I}_{00}$ is non-zero, and $\mathcal{C}_{\theta 00}^{\mathrm{TE}} = \mathcal{C}_{\phi 00}^{\mathrm{TM}} = 0$. Separating the AF in (5.8), the AIAA far-field contribution can be extracted from the AIUC ($\boldsymbol{E}_a$) operating inside a fully excited array environment (at a given P_{avs})

$$\boldsymbol{E}_a(r,\theta,\phi) = j\frac{\sqrt{\zeta_0 d_x d_y\cos\theta}}{\lambda}(\mathcal{A}_{00}^{\mathrm{TM}}\hat{\theta} - \mathcal{A}_{00}^{\mathrm{TE}}\hat{\phi})\frac{\exp\{-jkr\}}{r}, \tag{5.15}$$

where $\zeta_0 = 120\pi\ \Omega$ is the intrinsic impedance of free space; $\hat{\theta}$ and $\hat{\phi}$ are the θ- and ϕ-axis unit vectors. The ASEP can be obtained through the angular-dependent $\boldsymbol{E}_a$. The active scan element pattern of the AIUC ($\boldsymbol{G}_a$) is now derived from the standard definition of the realized gain for a passive unit cell [86], [89]. Recalling that $\mathcal{A}_{00}^{\mathrm{TE/TM}}$ depends on P_{avs}, the AIUC gain pattern can be expressed as

$$\boldsymbol{G}_{\mathrm{a}}(\theta,\phi,P_{\mathrm{avs}}) = \frac{4\pi d_x d_y\cos\theta}{\lambda^2}\left(\boldsymbol{G}_{\mathrm{T}}^{\theta}(\theta,\phi,P_{\mathrm{avs}})\hat{\theta} + \boldsymbol{G}_{\mathrm{T}}^{\phi}(\theta,\phi,P_{\mathrm{avs}})\hat{\phi}\right). \tag{5.16}$$

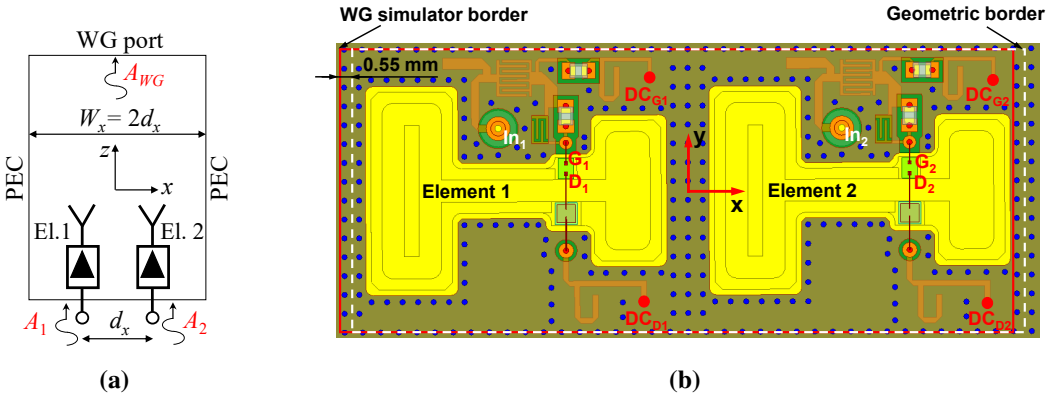


Figure 5.2: (a) Sketch of the two-element H-plane active infinite array WG simulator. (b) Top view of the two-element structure inside the WG simulator, indicating the WG cross-section (red solid) and the periphery (white dash) of two AIUCs.

The ASEP takes into account the AIUC transducer gain $G_{\mathrm{T}}^{\theta/\phi} = P_{00}^{\mathrm{TM/TE}}/P_{\mathrm{avs}}$ of the integrated PA and the radiating property of the AIUC. Hence, the ASEP accounts for both antenna and PA effects, including PA gain compression and its susceptibility to load mismatch.

5.2 Characterization of AIUC

Active infinite array Waveguide Simulator Technique

infinite array WG simulators can be applied to evaluate the performance of an infinite array for beam steering in various discrete conditions. These conditions are defined by the excited waveguide mode and the configuration of the AIAA elements placed inside the rectangular WG. Those elements are excited in such a way that each AIUC experiences the same EM conditions as in an infinite array environment for a specific beamsteering direction [90].

The relevant active infinite array WG simulator principles are as follows:

1. Although two plane waves are necessary to describe the TE_{10} dominant mode, four plane waves are required for higher-order modes that possess variations in both transverse directions [89], [90]. If the TE_{10} mode is excited, the infinite array WG simulator provides a condition equivalent to an AIUC dual-beam operation in H-plane at $\pm\theta_{\mathrm{g}}$ direction. The beamsteering angle, relative to the axis of the WG, can be obtained by [90]

$$\sin\theta_{\mathrm{g}} = \frac{\lambda}{\lambda_c} = \frac{\lambda}{2L_{\mathrm{WG}}} = \frac{\lambda}{4d_x}, \tag{5.17}$$

where the λ_c is the cutoff wavelength of the TE_{10} mode in the waveguide and λ is the free-space wavelength. After applying the unit cell symmetry property [91], it arrives at $\Gamma_{\mathrm{D1,2}} = \Gamma_{\mathrm{D}}(\theta_s = \theta_{\mathrm{g}}, \phi_s = 0°)$, where $\Gamma_{\mathrm{D1,2}}$ denotes the scan reflection coefficient (at the

drain port) of the two AIUCs inside the WG.

2. The AIUCs are to be excited with proper amplitudes $\mathcal{A}_i$ ($|\mathcal{A}_i| = \sqrt{2P_{\text{avs},i}}$, $i = 1, 2$) to generate the desired WG modal content. This can be represented mathematically, considering the relations specified above

$$\mathcal{A}_i = \mathcal{A}_{\text{FL}} \left[\exp\{-jkx_{ci}\sin\theta_{\text{g}}\} + \exp\{jkx_{ci}\sin\theta_{\text{g}}\}\right], \tag{5.18}$$

where $\mathcal{A}_{\text{FL}} = \sqrt{2P_{avs}}$ is the magnitude of the incident AIUC voltage wave for beamsteering to $\pm\theta_{\text{g}}$; x_{ci} is the radiation center of the i-th AIA element in x-axis. Substituting $x_{c1/2} = \pm d_x/2$ (Fig. 5.2a), one can find $A_1 = A_2 = 2A_{\text{FL}}\cos(kd_x\sin\theta_{\text{g}}/2)$. This finding is important since it ensures that both AIUCs will be under the same operational (or compression) condition.

The AIUC amplification gain is defined with the co- and cross-polarized field components of the fundamental Floquet modes ($P_{00}^{\text{co/xp}}$)

$$G_{\text{T}}^{\text{co/xp}} = \frac{P_{00}^{\text{co/xp}}}{P_{\text{avs}}}, \quad G_{\text{P}}^{\text{co/xp}} = \frac{P_{00}^{\text{co/xp}}}{P_{\text{in}}}, \tag{5.19}$$

where P_{avs} and $P_{\text{in}} = P_{\text{avs}}(1 - |\Gamma_{\text{in}}|^2)$ are the average available and accepted power at the input, respectively.

3. The position of the WG sidewalls shall coincide with the AIAA planes of symmetry (E-field null-planes) [90]. If the AIUC is perfectly geometrically symmetric, the AIUC's radiation and geometric center coincide. However, this design example slightly violates the symmetry requirement in the yz-plane due to the different shapes of the y-directed slots (see Fig. 5.1b). Consequently, the AIUC's radiation center is shifted in the x-axis direction by 0.55 mm relative to the geometric center. To realize symmetric fields, the WG is shifted accordingly to compensate for the difference between the two centers (see Fig. 5.2b).

Validation of Active infinite array Waveguide Simulator

The AIUC design example of a two-element H-plane infinite array WG simulator (Fig. 5.2a) is manufactured and characterized. The WG cross-section is measured as $L_{\text{WG}} = 2d_x$ and $W_{\text{WG}} = d_y$, where d_x and d_y are the element spacings in H- and E-plane, respectively. Fig. 5.3 presents a good agreement between the measured and simulated large-signal results, validating the active infinite array waveguide simulator as a practical approach to experimentally verify the EM and nonlinear behavior of a large-scale AIAA with affordable cost and time.

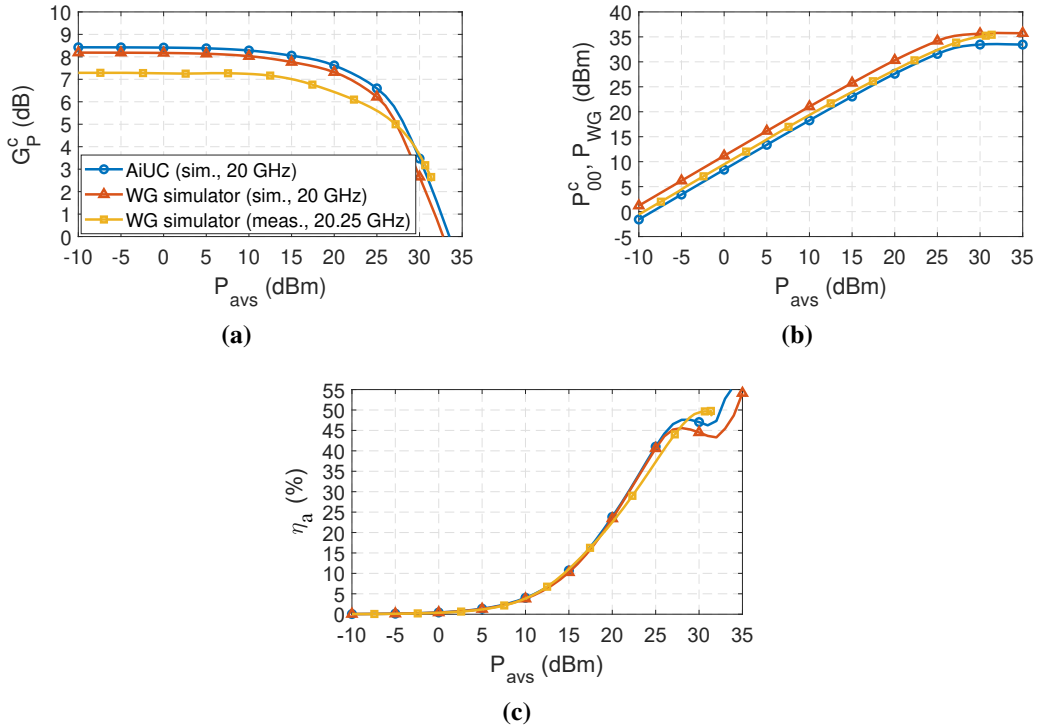


Figure 5.3: Large-signal performance of the AIUC in the infinite array environment $(\theta_s, \phi_s) = (23.7°, 0°)$ and when simulating the environment with the two-element active infinite array WG simulator: (a) power gain, (b) radiated power, and (c) AIUC power efficiency (6.6) of the co-polarized field component.

5.3 Conclusion

The active integrated unit cell design example—a two-element H-plane active infinite array waveguide simulator—has been manufactured and experimentally verified. A good agreement between the simulated AIUC and measured active infinite array waveguide simulator results in the large-signal regime has been observed. The discrepancy of the power gain and radiated power is around 1 dB and 2 dB, respectively. It confirms that the active infinite array waveguide simulator technique is a cost-effective and practical method to experimentally verify characteristics such as power efficiency, power gain and radiated power of active integrated antenna elements in infinite array scenarios.

The primary focus of improvement is to increase the bandwidth while keeping the power efficiency above 25%. An AIA element design integrated with a custom-designed PA MMIC that aims to increase the bandwidth to at least 10% at the center frequency $f_0 = 28$ GHz is detailed in the following chapter.

CHAPTER 6

KA-BAND WIDEBAND INTEGRATED ACTIVE ARRAY ANTENNAS

This chapter presents an integrated active array antenna element modified from the previous design example to operate at a higher center frequency 28 GHz and have an improved relative bandwidth of 11.3%. The power amplifiers are custom designed in GaN[1] 0.15 µm and GaAs[2] processes for improved integration level and performance. A contactless PA-antenna transition is introduced to enable the broader bandwidth and reduce the losses at the interconnection. The active integrated unit cell of an infinite array of such elements integrating the PA MMIC and the modified cavity-backed slot radiator through the contactless interconnection has been simulated. An active infinite array waveguide simulator has been manufactured and employed to experimentally verify the behavior of an infinite array of the AIUC as a function of scan angle and available input power.

6.1 Monolithic Microwave Integrated Circuit

Power Amplifier Design

Two PA MMICs in GaN[1] and GaAs[2] processes are custom designed for integrating into the AIA element in order to provide enhanced performance. The PA designs are based on the design specification in Table 3.1, and the joint design flow (Section 3.1) is utilized to decide the optimal interface impedance and make design trade-offs at the system level.

[1] WIN Semiconductor NP15-00 0.15 µm 28 V Operation GaN HEMT process.
[2] WIN Semiconductor PIH1-10 4 V GaAs *p*HEMT MMIC Technology.

GaN PA

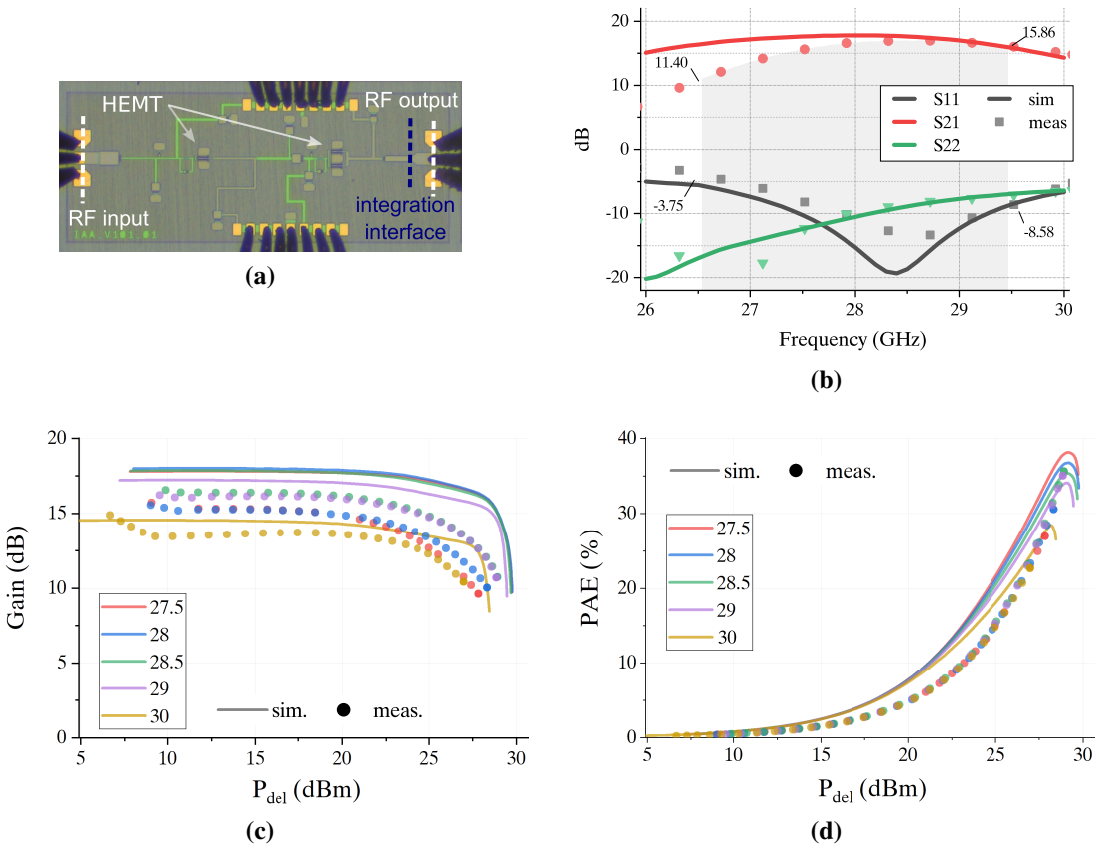


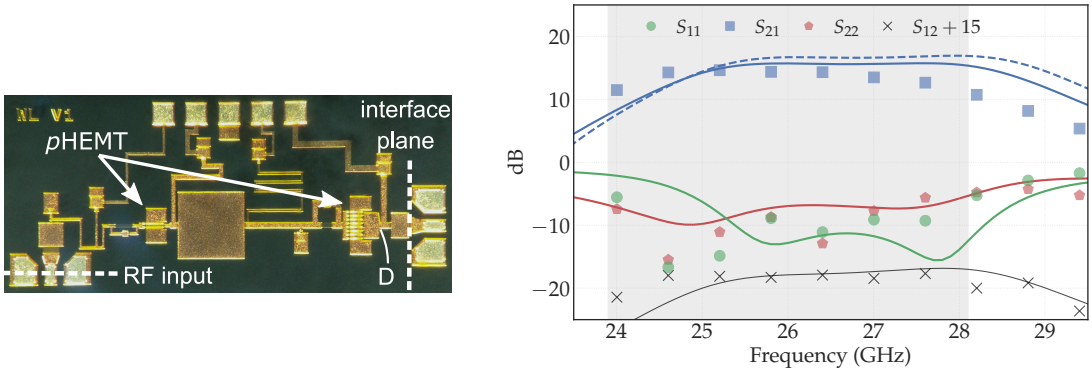
Figure 6.1: (a) Micrograph of the fabricated two-stage GaN PA (2.95 mm × 1.1 mm). Measured and simulated (b) *S*-parameters and large-signal PA behavior on (c) transducer gain and (d) PAE with 50 Ω load ($Z_o = 50\ \Omega \neq Z_{L,f_0}^{\text{opt}}$).

A two-stage PA developed in the GaN process is fabricated and shown in Fig. 6.1a. The PA output is not transformed to 50 Ω due to applying the direct integration technique. The device is on-wafer tested with 50 Ω port at the input and output. Hence, the measurement results are to verify the foundry design kit, and the optimal characteristics with optimal PA loading are not tested. The small-signal behavior presented in Fig. 6.1b shows a good agreement between the simulated and the measured S-parameters (both with 50 Ω reference impedance) from 28 GHz to 30 GHz, where the transmission coefficients differ less than 0.5 dB. The discrepancy of the simulated and measured $|S_{21}|$ at 26 GHz is caused by the impedance mismatch at the input and output ports (reference planes at the ground-signal-ground (GSG) pads in Fig. 6.1a). Fig. 6.1c presents the measured operating power gain in the large-signal regime. Similarly, a gain discrepancy of less than 2 dB in large-signal measurements is observed at most frequencies except 26 GHz. The measured PAE in Fig. 6.1d demonstrates a peak efficiency >30% between 28 GHz and 29.5 GHz. It is worth noting that the small- and large-signal results are not characterized

with the optimal PA loading condition, i.e., $Z_L = 32\,\Omega$. Therefore, higher power gain, saturated output power, and PAE can be expected when the PA is tested with the optimal output loading rather than with a 50 Ω load. Despite minor discrepancies between simulations and measurements, the characteristics of the GaN PA MMIC are promising to meet the design specification in Table 3.1, e.g., $P_{\text{out}} \geq 15\,\text{dBm}$ and the total power efficiency ≥25%. Although the measured impedance bandwidth is narrower than the expected 10%, the performance in the 26–27 GHz band can be improved by adjusting the input impedance matching of the PA design based on the discrepancy between the simulations and measurements.

Although the GaN PA design demonstrates high power and efficiency suitable for AIA integration, the final PA design has been migrated to the GaAs process since the GaN process is temporarily unavailable after the first tape-out.

GaAs PA



(a) **(b)**

Figure 6.2: (a) Micrograph of the fabricated GaAs PA with GSG pads at the input and output for characterization (2 mm × 0.9 mm). (b) Small-signal: characterized with 50 Ω load (symbols), and numerical results shown for 50 Ω load (solid) and the optimal load $Z^{\text{opt}}_{L,fo} = 20\,\Omega$ (dashed).

A two-stage GaAs *p*HEMT PA has been designed in ADS circuit simulator with the transistor model along with the design kit provided by the foundry. The PA input is matched to 50 Ω, and the direct integration technique is to be applied at the output. To satisfy the design system specifications (Table 3.1), the optimal load condition (reference plane D in Fig. 6.2a) is $Z^{\text{opt}}_{D,f_0} = 9.7 + j10.4\,\Omega$ at the fundamental frequency $f_0 = 28\,\text{GHz}$, where $|\Gamma^{\text{opt}}_D(2f_0)| \geq 0.95$ and $\angle\Gamma^{\text{opt}}_D(2f_0) \approx 0°$ for the $8 \times 50\,\mu\text{m}$ GaAs *p*HEMT[1] implemented in the second stage. The PA operates in class AB for a trade-off between the linearity and PAE. Although Doherty amplifiers offer high PAE in exchange for poor linearity, they are not in the scope of this thesis due to the need of computationally expensive DPD algorithms for linearization. The bias line of the drain is used to resonates out the parasitic capacitance at the transistor output. Therefore, the optimal

[1] $8 \times 50\,\mu\text{m}$ represents 8 gate fingers with the gate width of 50 µm.

load impedance becomes $Z_{L,f_0}^{\text{opt}} = 20\ \Omega$ at the interface plane, with only the resistance left for the antenna to match. This technique simplifies the antenna design, and a wider bandwidth in terms of the antenna's active impedance has become easier to attain.

Fig. 6.2a presents a micrograph of the two-stage GaAs PA. This PA is characterized on-wafer using the MPI TS150-THZ probe station. No impedance tuner is utilized in the characterization; therefore, both the input and output ports are tested with 50 Ω ports. The small-signal measurement is plotted in Fig. 6.2b. A frequency shift (around 1 GHz) is observed between the measured and simulated *S*-parameters, which is caused by the transistor model used in the circuit simulation. Nonetheless, the large-signal results (Sec. 6.6, Fig. 6.11) show that this *p*HEMT model provides sufficient accuracy in the large-signal regime, thus, good agreements between the simulations and measurements. However, the discrepancy in S_{22} indicates that the PA output impedance is different from the simulated value, which can impact the PA characteristics when directly integrated with the radiating element. The simulated results of the PA with the optimal output loading $Z_{L,fo}^{\text{opt}} = 20\ \Omega$ are also plotted for comparison, which shows a 3 dB bandwidth of 15% (23.9–28.1 GHz).

6.2 Contactless Transition

Wire bonding is commonly used to interconnect ICs to off-chip components or antennas as implemented in the previous designs (Chapter 3, Chapter 5). An on-chip radiating element (or probe) can couple to an external superstrate (EM-coupled) [92]–[94], dielectric resonator/lens (field-integration) [20], [95]–[98], or directly radiate in free space (AoC without integrated to off-chip component) [99]–[102]. Nevertheless, these methods have considerable shortcomings. Bond wire interconnection increases the complexity and uncertainty during assembly due to its low repeatability. It also limits the bandwidth and increases the insertion loss at high frequencies because the inductance varies drastically as the wire length changes [32]. Superstrates and dielectric resonators and lenses are relatively costly due to the design complexity of custom-designed parts. The radiation efficiency of AoCs can still be suboptimal, even integrated with those additional parts to boost it. Moreover, lenses and superstrates generally have sizeable form factors [20], [92], [94], [98], [103], which increases the inter-element spacing, resulting in the occurrence of grating lobes at low scan angles.

A contactless EM-coupling transition is proposed to provide a high efficient broadband interconnect solution by coupling the PA output through an E-plane open-loop probe, which is integrated onto the PA MMIC, to the cavity-backed slot radiator (Fig. 6.3). The interface plane for direct integration is defined at the output DC block, as shown in Fig. 6.3d. The backside MMIC metallization underneath the probe region was removed (Fig. 6.3c) to prevent the probe field shielding. The probe primarily couples to the slot's E-field, whereas the open-loop shape allows for a reduced footprint. From the EM perspective, the open-loop probe represents an impedance transformer with a series reactance [104]. Consequently, the radiating element combined with the on-chip probe transition alleviates the difficulty of impedance matching to a wide

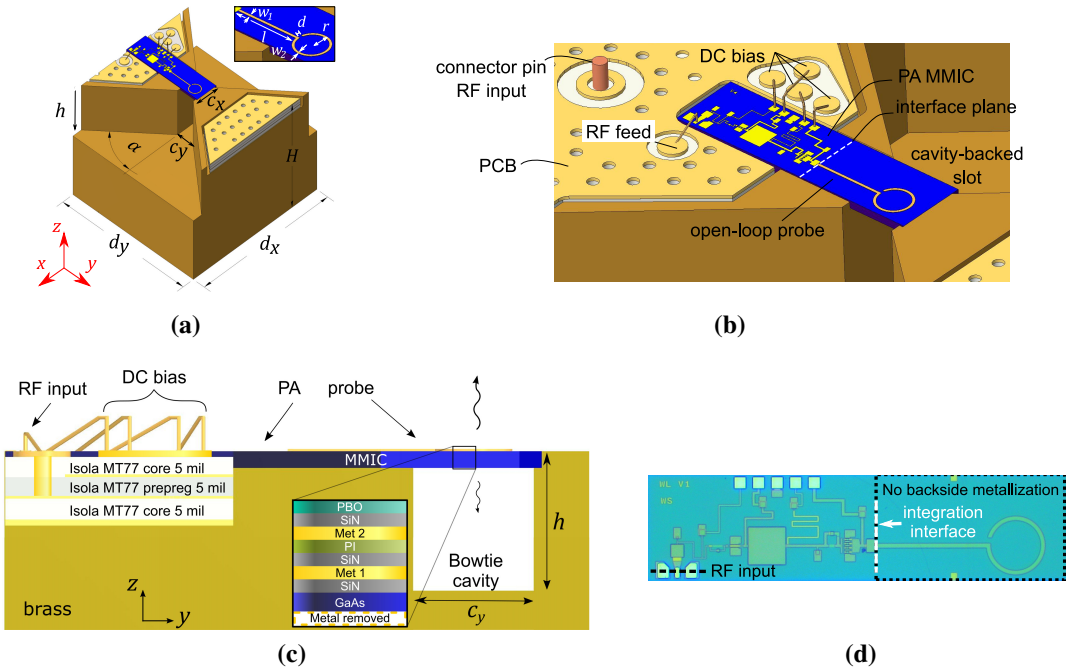


Figure 6.3: (a) The proposed AIUC in 3D view (unit: mm). (b) A close-up in the middle section of the AIUC. The open-loop probe connected to the PA output for EM coupling to the cavity-backed slot radiating element. The backside MMIC metallization beneath the probe is removed to avoid obstructing the coupling and radiation. (c) The cross-section side view of the AIUC in the hybrid integration environment. The dual-stage PA is designed in the GaAs *p*HEMT technology and integrated with an on-chip E-plane probe for EM coupling to the slot radiator. The input signal and DC bias are fed through bond wires. (d) A micrograph of the MMIC PA and on-chip probe .

bandwidth with respect to the optimal load impedance (detailed in the next section).

The proposed on-chip contactless transition offers a power-efficient solution, lessens the limitation on the bandwidth and brings assembly complexity down, and may therefore represent a cost-effective solution, provided that the increased chip area is acceptable.

6.3 Radiating Element

The GaAs PA MMIC in Sec. 6.1 demonstrates a 3 dB bandwidth of 15%. Similarly, it is desired to have a radiating element with at least 10% targeted bandwidth. The initial AIA design examples in Chapter 3 and Chapter 5 are narrowband[1] (<2%), partly caused by the frequency-dependent resonant slot radiating elements. Hence, the radiating element of the previous design has been modified to a cavity-backed *bowtie* slot for its broadband frequency response [105], with an increased center frequency of 28 GHz. It is worth mentioning that the mutual coupling effects (at least in theory) in arrays are generally minimized to provide better isolation between the interconnected amplifiers. Nonetheless, a high mutual coupling level can also be leveraged

[1] In terms of the power efficiency more than 20%.

for wideband and wide-angle ($\pm 40°$) scanning array designs by exploiting the connected arrays [106]–[108]. In this work, the bowtie slot elements (Fig. 6.3a) are connected in the H-plane ($xz-$plane) and no longer narrowband frequency-dependent resonators, where the electric current distribution across the array becomes more continuous [106]. The radiating structure is CNC-milled from brass alloys for attaining high radiation efficiency[1] (>93%) and high thermal conductivity, which is favorable considering a substantial amount of heat is dissipated from large-scale PA arrays.

The optimal antenna impedance (for direct integration) is the outcome from the AIA design parameters (output power, power gain, PAE, and linearity) and the trade-offs made in the antenna-circuit co-design flow (Fig. 3.1). In this design, the optimal PA loading that satisfies the design specification (Table 3.1) has been obtained from the GaAs PA design in Sec. 6.1, i.e., $Z^{\text{opt}}_{L,f_0} = 20\,\Omega$. Since the EM-coupling transition and the radiating element are a unified design, they need to be co-designed and co-optimized to realize the desired antenna impedance. To this end, a full-wave model of the AIUC passive components, including the cavity-backed bowtie slot radiator, the GaAs on-chip probe, the PCB, and the connector launch pin (See Fig. 6.3b), are simulated in Ansys HFSS EM solver. An input port with 20 Ω reference impedance is introduced at the interface plane. A Floquet port and periodic boundary conditions are assigned in the AIUC model. This passive AIUC design has been optimized for the widest scan range with at least 10% targeted bandwidth by minimizing the active reflection coefficient (Γ_L) at the input port. The final design parameters were found as follows (Fig. 6.3a): The probe consists of a microstrip line with the length $l = 898\,\mu\text{m}$ and width $w_1 = 35\,\mu\text{m}$ and an open loop with the radius $r = 236\,\mu\text{m}$, width $w_2 = 30\,\mu\text{m}$, and gap $d = 45\,\mu\text{m}$. The cavity-backed bowtie slot radiator has a flare angle $\alpha = 49.5°$, E-plane size $d_y = 5.73\,\text{mm}$, H-plane size $d_x = 5.98\,\text{mm}$, and a center slot section with the width $c_x = 0.92\,\text{mm}$ and length $c_y = 0.74\,\text{mm}$. The slot depth is chosen to be h =2.16 mm, slightly shallower than a quarter-wavelength at $f_0 = 28\,\text{GHz}$, which is utilized to provide an inductive slot reactance to compensate the open loop capacitance.

Fig. 6.4a shows the simulated Γ_L 2-D frequency-scan-angle maps ($Z_0 = Z^{\text{opt}}_{L,f_0} = 20\,\Omega$) of the AIUC radiating element, including the effects of the on-chip probe and the cavity bowtie slot radiator, which demonstrates an impedance bandwidth of 16.4% at broadside radiation ($\Gamma_L \leq -8\,\text{dB}$, 25.3–29.8 GHz), where $\Gamma_L \leq -8\,\text{dB}$ provides sufficient impedance matching to deliver targeted large-signal PA performance. Fig. 6.4b and 6.4c plot the active reflection coefficient during beamsteering in the Smith chart for the E-plane and H-plane, respectively. The normalized co- and cross-polarized scan element patterns in two principal planes are simulated and presented in Fig. 6.4d and 6.4e, along with the onset of the grating lobe illustrated with dotted lines. It is observed that in the E-plane (yz-plane), the AIUC experiences scan blindness, occurring near the onset of the grating lobe. Nonetheless, this phenomenon is not seen in the H-plane (xz-plane).

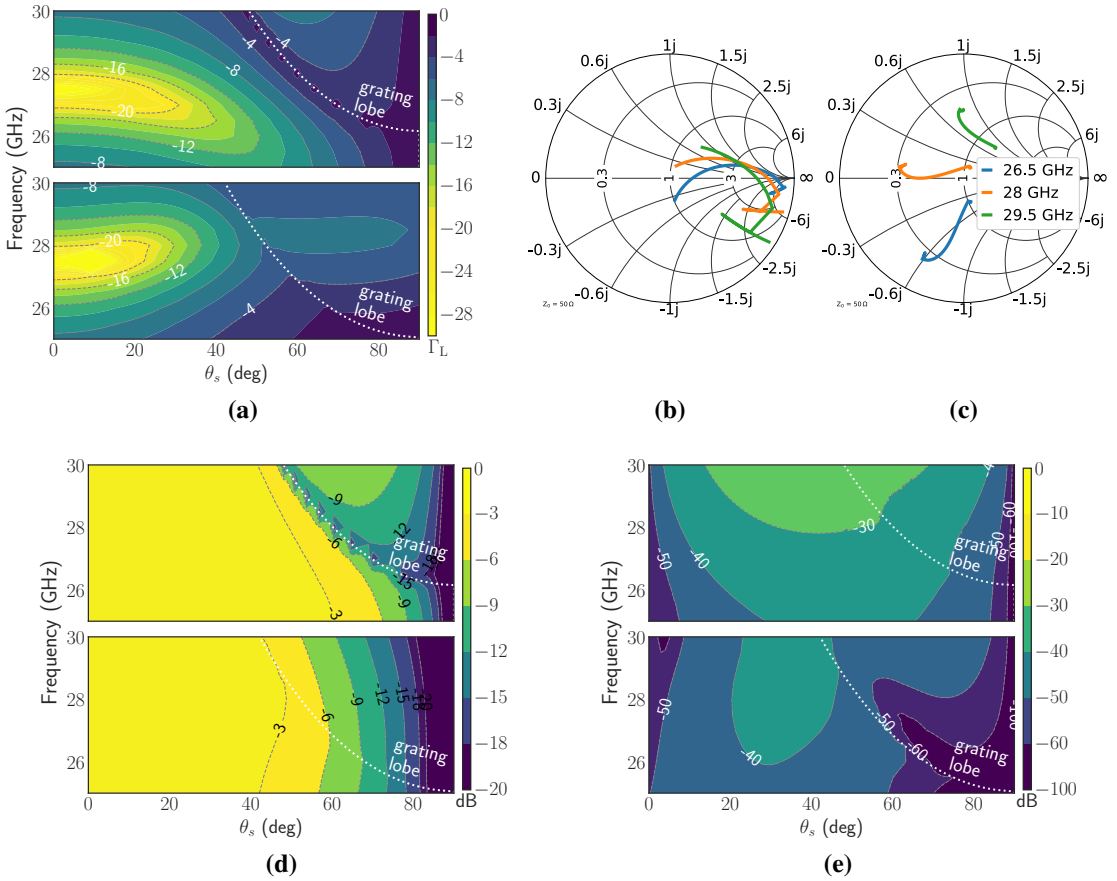


Figure 6.4: (a) The active reflection coefficient of the AIUC passive radiating part at the integration interface plane (see Fig. 6.3d) for beamsteering in the E- (*top*) and H-plane (*bottom*), with respect to the optimal load impedance $Z^{\text{opt}}_{L,f_0} = 20\ \Omega$. Γ_L during beamsteering ($Z_0 = Z^{\text{opt}}_{L,f_0} = 20\ \Omega$) in (b) the E-plane and (c) H-plane. The simulated normalized (d) co- and (e) cross-polarized scan element patterns of the AIUC passive radiating structure (slot radiator and the MMIC probe, see Fig. 6.3a) in the E- (*top*) and the H-plane (*bottom*) in the 25–30 GHz range. The onset of grating lobes is shown by dotted lines.

6.4 Broadband Active Integrated Unit Cell

The AIUC of integrated infinite array antennas is developed by combining the components from the previous sections. Fig. 6.3 shows the AIUC design configuration, comprising the cavity-backed bowtie slot radiator, the GaAs PA MMIC, the on-chip probe for transition, and the multi-layer PCB for signal feed and DC bias. The whole model is co-simulated in the combined EM-circuit solver (Sec. 3.1). The cross-section side view of the AIUC design (Fig. 6.3c) illustrates how the PA MMIC and on-chip probe, the PCB, and the bowtie slot radiator are co-integrated in the AIUC. The PA is fed from the PCB via bond wires for both RF and DC, and the probe, integrated into the PA output DC block, couples to the slot radiating element. The AIUC periphery

[1] Simulated results.

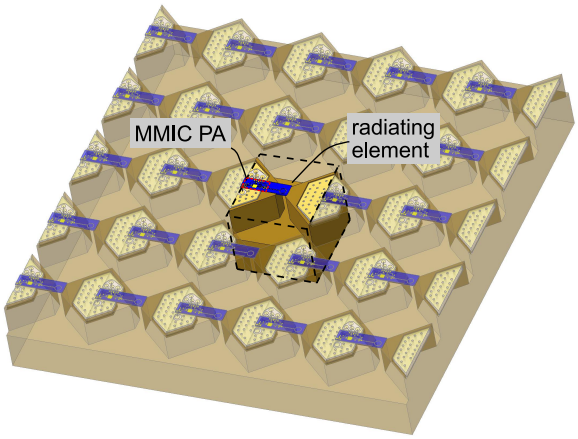


Figure 6.5: A fragment of the planar active integrated array antenna of bowtie connected-slot radiating elements with integrated MMIC PAs. A single AIUC is highlighted.

measures[1] $0.56\,\lambda \times 0.54\,\lambda \times 0.2\,\lambda$ (length×width×depth), which is considered a compact AIA element design applicable to wide-angle (±40°) scanning arrays. The unit cell is designed by including 42 Floquet modes that propagate at the third harmonic frequencies $3f_0$ to ensure accurate large-signal analysis in ADS Harmonic Balance simulation. A fragment of the planar active integrated array antenna of bowtie connected-slot radiating elements with integrated MMIC PAs is illustrated in Fig. 6.5.

6.5 Beamsteering Performance

The AIUC performance metrics in terms of the active scan element pattern (ASEP), power efficiency, and EIRP are defined and implemented to evaluate the beamsteering performance in this section. The ASEP, utilized to quantify the active antenna gain, is defined as in (5.16)

$$\boldsymbol{G_a}(\theta,\phi) = \frac{4\pi d_x d_y \cos\theta}{\lambda^2}\left(G_{\mathrm{T}}^{\theta}(\theta,\phi)\hat{\boldsymbol{\theta}} + G_{\mathrm{T}}^{\phi}(\theta,\phi)\hat{\boldsymbol{\phi}}\right) \tag{6.1}$$

where the power dependence is assumed and (θ,ϕ) indicate the radiation direction. Similarly, the angle-dependent AIUC power efficiency is represented as

$$\eta_a(\theta,\phi) = \eta_{\mathrm{D}}(\theta,\phi)\eta_{\mathrm{rad}}(\theta,\phi) = \frac{P_{\mathrm{TE/TM_{00}}}}{P_{\mathrm{DC}}} \tag{6.2}$$

where $P_{\mathrm{TE/TM_{00}}}$ is the power radiated by the fundamental Floquet modes. The AIUC EIRP can be expressed by

$$\mathrm{EIRP}(\theta,\phi) = P_{\mathrm{avs}}\boldsymbol{G_a}(\theta,\phi), \tag{6.3}$$

[1] λ represents the wavelength of the center frequency.

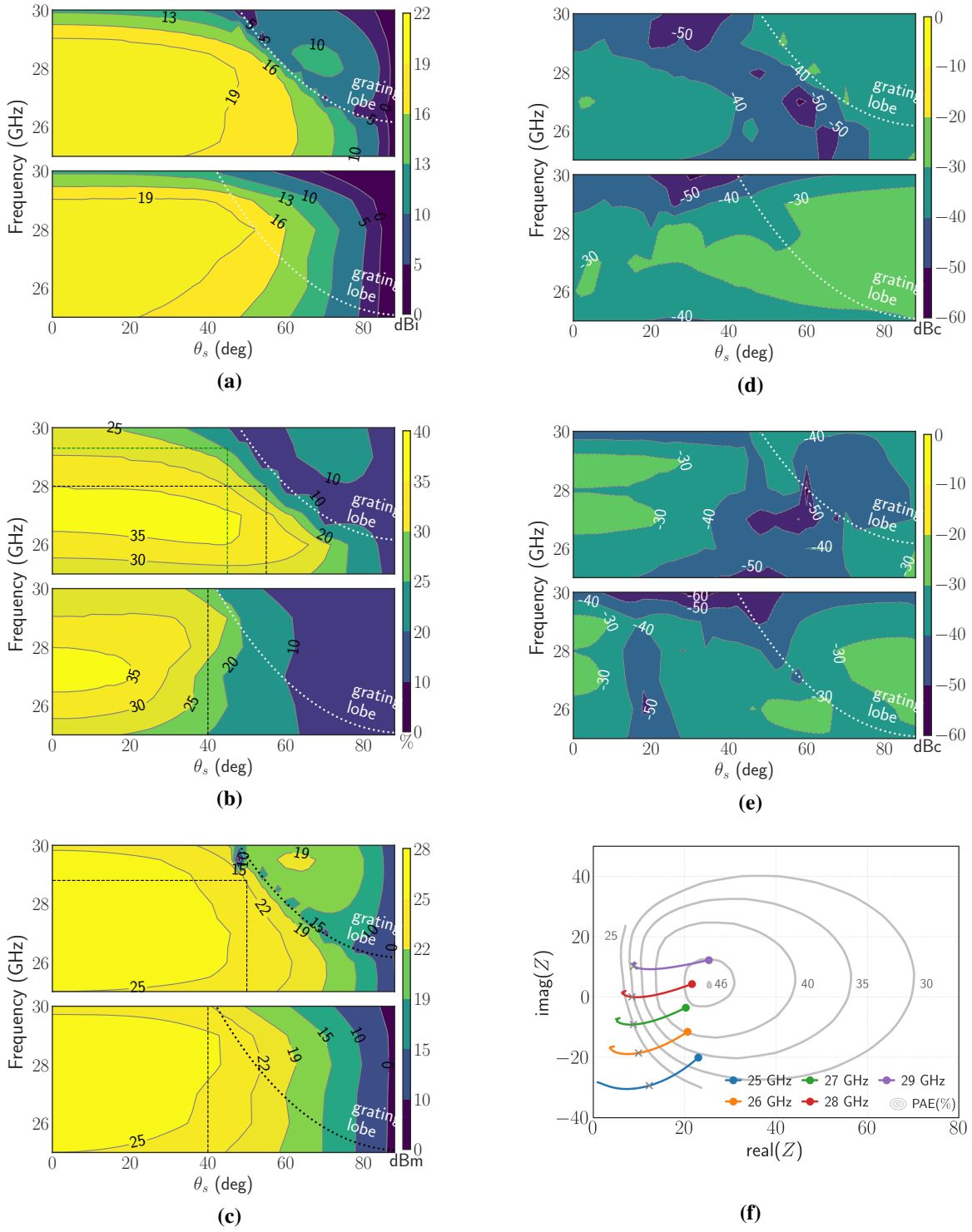


Figure 6.6: AIUC's (a) active antenna gain, (b) power efficiency, (c) EIRP, and (d) second- and (e) third-order harmonic distortion for beamsteering at θ_s direction in the E-plane (*up*) and H-plane (*bottom*) when operating at P1dB. (f) The load-pull for maximum PAE ($f_0 = 28\,\text{GHz}$) and the active radiating element impedance for $\theta_s = 0°$ to 90° in the H-plane. Markers indicate the broadside ($\theta_s = 0°$) and $\theta_s = 45°$ directions.

where the PA amplification and nonlinear effects and the radiating element's radiation property are considered in $G_a(\theta,\phi)$ term.

Fig. 6.6 presents the AIUC beamsteering performance in an infinite array scenario when operating at the P1dB level. The AIUC can scan up to 40° in both principal planes with a maximum gain scan loss of 3 dB. When taking efficiency as the criterion, i.e., $\eta_a \geq 20\%$ (design constraints in Table 3.1 with adjustment), the E-plane scan range is ±55° with a fractional bandwidth of 11.3% (25–28 GHz), as shown in Fig. 6.6b. When reducing the scan range to ±45°, the bandwidth is increased to 15.8% (25–29.3 GHz). In the H-plane, the scan range is around ±40° at 25–30 GHz band. The EIRP result (Fig. 6.6c) shows a ±50° scan range (14.1% FBW, 25–28.8 GHz) and ±40° (25–30 GHz) for each principal plane when EIRP ≥22 dBm.

The scan range in the E-plane (with η_a criterion) is mainly confined by the scan blindness near the onset of the grating lobe, which exacerbates at higher frequencies. In the H-plane, η_a drops more drastically as θ_s increases compared to the E-plane. The power efficiency significantly deteriorates when $\theta_s > 45°$, even though no scan blindness occurs in this plane. Fig. 6.6f, where the active impedance of the radiating element and the simulated load-pull are overlapped in the plot, explains this phenomenon. The real part of the active impedance decreases as the scan angle (θ_s) increases, corresponding to a significant decline in PAE when θ_s>45°.

To ensure PA linearity and delivered output power at the fundamental frequency, harmonic distortion (HD) is investigated. Second-order harmonic distortion HD_2 is the power level of the second-order harmonic with respect to the fundamental frequency. The second and third-order harmonic distortions are obtained as

$$HD_2 = \frac{P^2_{TE/TM_{00}}}{P_{TE/TM_{00}}}, \quad HD_3 = \frac{P^3_{TE/TM_{00}}}{P_{TE/TM_{00}}} \tag{6.4}$$

where $P^{2/3}_{TE/TM_{00}}$ are the second- and third-order harmonic power levels of the TE_{00} and TM_{00} Floquet modes. Fig. 6.6 shows that both HD_2 and HD_3 are at least 20 dB below the fundamental power for all scan angles (θ_s) in both principal planes. These results clearly show that a large-scale array of such AIUCs is less likely to suffer from harmonic and intermodulation distortions in beamsteering conditions.

6.6 Experimental Results

Active Infinite Array Waveguide Simulator

The active infinite array WG simulator for "single"-AIUC has been developed and manufactured to experimentally verify the PA characteristics and radiation property of the AIUC. The exploded view of the active WG simulator is presented in Fig. 6.7a. Fig. 6.7b shows the WG cross-section and the off-chip components, including the lumped components for bypass circuits and the IMN between the *K*-connector and the bonding pad for MMIC feeding. The layout of the PCB inner layers and the schematic of the RF bypass circuit are depicted in Fig. 6.7c and 6.7d.

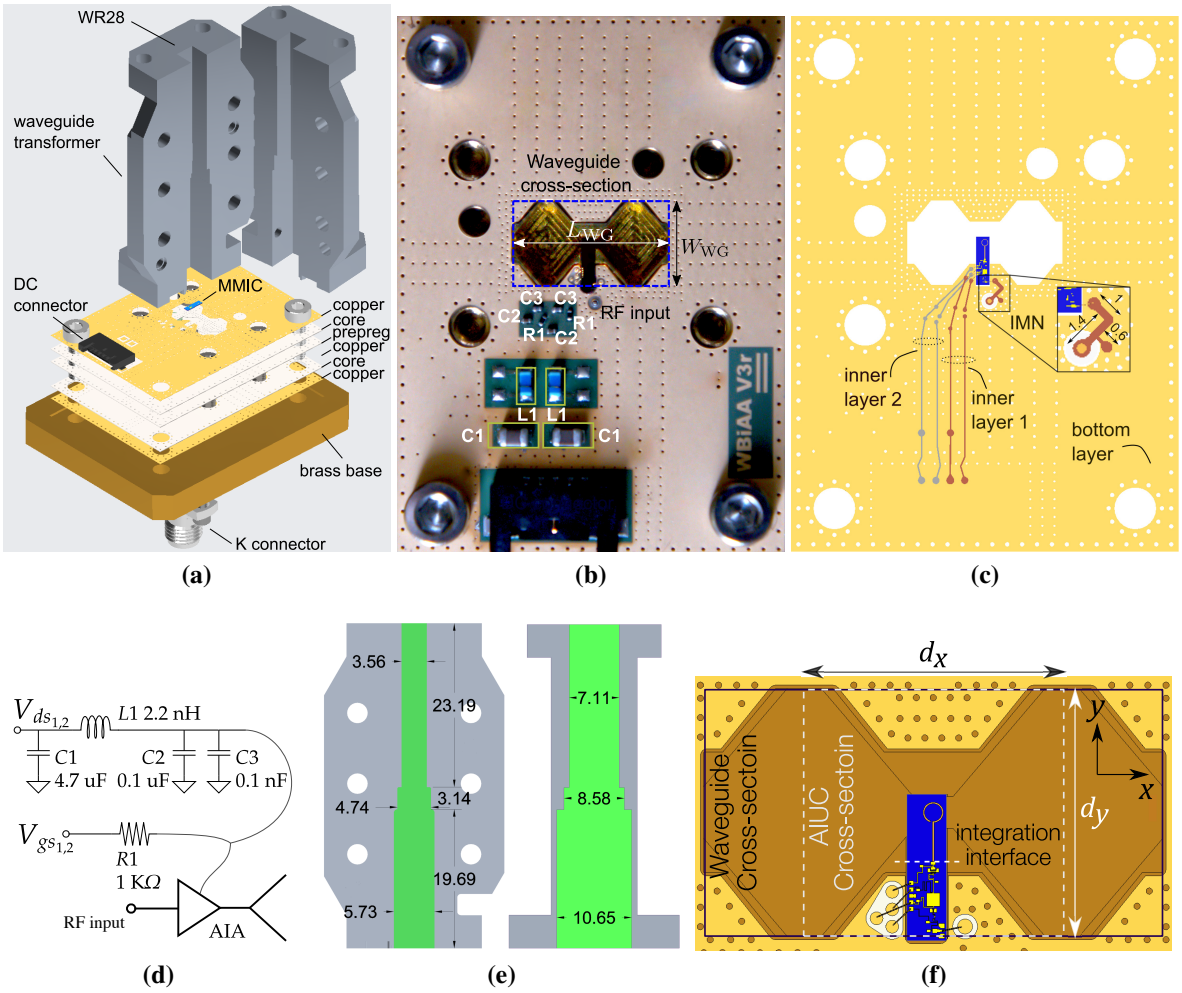
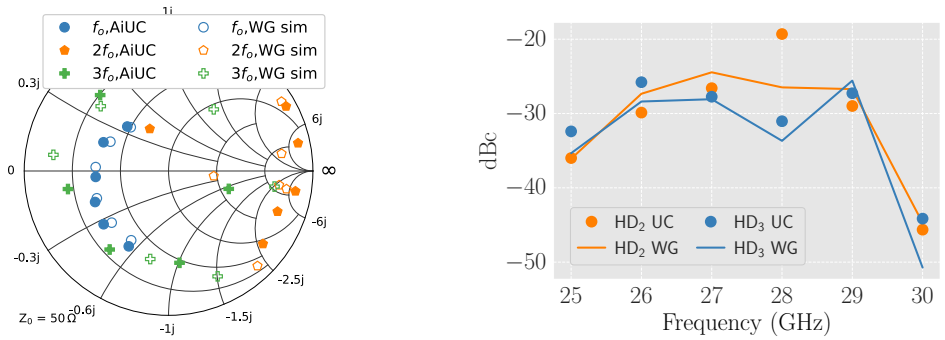


Figure 6.7: Design of the active infinite array WG simulator for experimental validation of the AIUC at beamsteering angle θ_g (6.7). (a) Exploded view of the active WG simulator prototype. (b) Design top view, denoting the cross-section of the WG ($L_{\text{WG}} \times W_{\text{WG}}$), the signal input, and the lumped components for bypass circuits. (c) PCB inner layers layout for off-chip DC bias, bypass circuit and IMN between the microwave connector and bonding pad (unit:cmm). (d) Schematic of the off-chip bypass circuit. (e) Side view of the WG transformer from $L_{\text{WG}} \times W_{\text{WG}}$ to WR-28 WG interface (unit: mm). (f) The AIUC and its cross-section, where d_x and d_y denote the element size in the H- and E-planes.

The WG cross-section is defined by $L_{\text{WG}} \approx 1.8 d_x$ and $W_{\text{WG}} = d_y$. The WG component includes a transformer section, transforming the WG cross-section to the WR-28 waveguide interface, as shown in Fig. 6.7e. The top view of the AIUC in the WG simulator is illustrated in Fig. 6.7f. A comparison of the simulated active reflection coefficient between the AIUC and the active infinite array WG simulator (with the same beamsteering angle) is presented in Fig. 6.8a. The transformer section of the WG part is employed to improve the impedance matching at the fundamental frequencies; therefore, the impedance of the AIUC and active WG simulator at these frequencies are very close, as observed in Fig. 6.8a. Nevertheless, the transformer also affects



(a) **(b)**

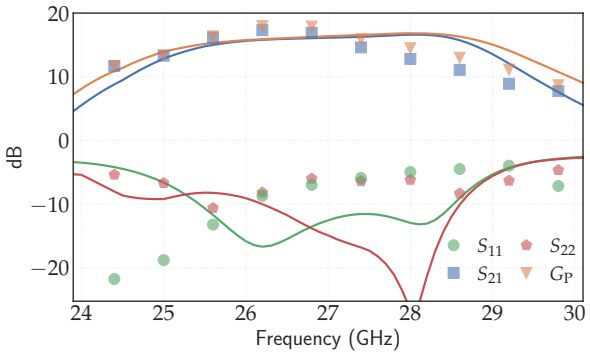
Figure 6.8: (a) Simulated active reflection coefficient Γ_L of the AIUC and active infinite array WG simulator (same beamsteering angle) at the fundamental frequencies ($f_0 = 25$–30 GHz) and higher-order harmonic frequencies $2f_0$ and $3f_0$. (b) Simulated second and third harmonic distortion of the AIUC and active WG simulator at 25–30 GHz.

the impedance matching at the second and third harmonic frequencies, leading to undesired discrepancies. Fig. 6.8b presents the second- and third-order harmonic distortions for both the AIUC and WG simulator are below -20 dBc. As can be seen later in this section, the simulated large-signal power efficiency and power gain of the AIUC and active infinite array WG simulator are almost identical (Fig. 6.11), which affirms that the impedance discrepancies at the second and third harmonic frequencies have negligible effects on the power efficiency and radiated power.

Small-Signal Characterization

The prototype of the active infinite array WG simulator is first characterized in the small-signal regime. The input and output ports of the AIUC, placed inside the active WG, are connected to a Keysight N5247A PNA using a 2.92 mm coaxial connector and a WR-28-to-2.92 mm waveguide adapter. Fig. 6.9 shows the small-signal measurement results, where the transducer gain ($G_{\mathrm{T}}^{\mathrm{CO}} = |S_{21}|$) and the power gain ($G_{\mathrm{P}}^{\mathrm{CO}} = |S_{21}|^2/[1-|S_{11}|^2]$) are in good agreement with the simulations. Nevertheless, the discrepancy in S_{22} at 26–28 GHz suggests that the active antenna impedance, i.e., the PA load impedance, differs from the PA optimal loading condition in this frequency band. The peak radiated power, power gain, and power efficiency of the AIUC at those frequencies can be influenced by the impedance mismatch at the interface plane, elaborated later in the large-signal characterization. The contributors to the active impedance mismatch include but are not limited to the manufacturing tolerance of the slot radiator (20–100 µm), the misalignment of the probe (50–200 µm) and the waveguide part (1–2 mm) relative to the slot.

The reflection coefficient shows a larger disagreement between measurements and simulations compared to the on-wafer characterized result. This finding indicates that additional impedance mismatching is introduced during the assembly procedure, likely caused by PCB permittivity variation, assembly and manufacturing tolerances, such as from the bond wire for signal feed, and the IMN between the microwave connector and bonding pad realized on PCB.



(a)

Figure 6.9: Measured (symbols) and simulated (solid lines) small-signal results for the AIA inside the active infinite array waveguide simulator.

Large-Signal Characterization

Metrics defined before are implemented herein to verify the AIUC performance in the large-signal regime. Furthermore, the polarization property of the radiating element is considered in the simulated and experimental results presented in this subsection. The AIUC operating power gain, accounting for the co-polarization efficiency of the radiating element, can be defined as

$$G_{\mathrm{P}}^{\mathrm{CO}}(\theta,\phi) = \frac{P_{\mathrm{del}}^{\mathrm{CO}}(\theta,\phi)}{P_{\mathrm{avs}}(1-|S_{11}|^2)} = \frac{P_{\mathrm{del}}^{\mathrm{CO}}(\theta,\phi)}{P_{\mathrm{in}}} = \frac{P_{00}^{\mathrm{CO}}(\theta,\phi)}{P_{\mathrm{in}}} = \frac{P_{10}^{g\mathrm{TE}}(\theta,\phi)}{P_{\mathrm{in}}} \tag{6.5}$$

where $P_{\mathrm{del}}^{\mathrm{CO}}$ represent the radiated (delivered) power, considering only the co-polarization field component, at the reference plane B in Fig. 6.10. $P_{\mathrm{del}}^{\mathrm{CO}}$ can be obtained from the power radiated by the fundamental Floquet modes (P_{00}^{CO}) or the waveguide dominant mode ($P_{10}^{g\mathrm{TE}}$). Similarly, the AIUC power efficiency taking accounts of the co-polarized field component is expressed by

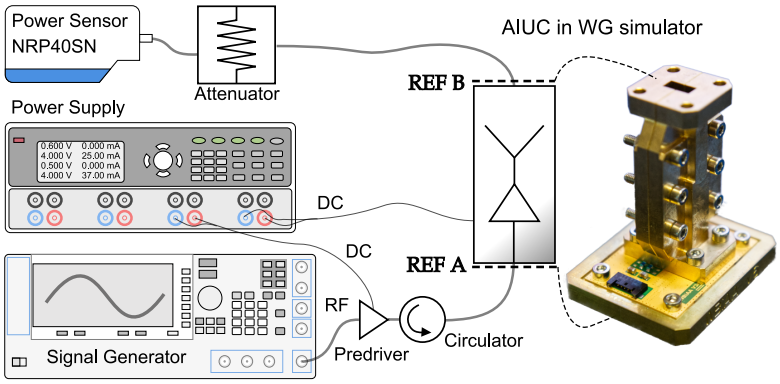
$$\eta_a^{\mathrm{CO}} = \eta_{\mathrm{D}} \cdot \eta_{\mathrm{rad}} \cdot \eta_{\mathrm{pol}} = \frac{P_{00}^{\mathrm{CO}}}{P_{\mathrm{DC}}} = \frac{P_{10}^{g\mathrm{TE}}}{P_{\mathrm{DC}}} \tag{6.6}$$

where η_{D} and η_{rad} are the PA drain efficiency and antenna radiation efficiency in (3.4). η_{pol} denotes the polarization efficiency, and P_{DC} represents the DC power consumption of the AIUC. Similar to (5.17), the beamsteering angle θ_g of the active infinite array WG simulator can be calculated by

$$\theta_g(f_0) = \arcsin\left(\frac{\lambda_o}{2L_{\mathrm{WG}}}\right) \approx \arcsin\left(\frac{c}{3.6 d_x f_0}\right). \tag{6.7}$$

where c is the speed of light in free space.

Characterization in the large-signal regime is indispensable to verify the power efficiency, peak radiated power, and linearity of the AIUC. The AIUC inside the active WG simulator emulates the EM and nonlinear conditions of an infinite array of such elements, beamsteering at θ_s direction in the H-plane. The measurement setup is depicted in Fig. 6.10. A PA predriver is



(a)

Figure 6.10: Concept of the measurement setup for large-signal characterization of the AIUC inside the active infinite array waveguide simulator.

used to increase the input available power (P_{avs} at ref. plane A in Fig. 6.10) to the desired range (-20 dBm to 20 dBm). Additionally, a circulator is connected between the predriver and the active WG simulator to bypass any reflected power due to impedance mismatch at the simulator input (ref. plane A). Both the AIUC and the predriver are DC-biased with a DC power supply, and a 10-dB attenuator is connected between the power sensor and the WG simulator output (ref. plane B) to avoid damaging the measurement equipment by power overloading.

Fig. 6.11 shows the simulated results of the power efficiency η_a^{CO} and power gain G_{P}^{CO} for the AIUC and the active WG simulator at various frequencies. A perfect agreement between the AIUC and the WG simulator results is noticeable, concluding that the impedance mismatch at higher harmonics has negligible effects on the performance. The measured result of the active WG simulator is also shown in Fig. 6.11, where the scan angle varies from 32° to 28° for frequencies at 27–29.6 GHz. The AIUC prototype demonstrates expected characteristics in the power gain and power efficiency overall. A maximum gain difference of 2.5 dB is observed, and the early gain compression at frequencies below 28 GHz is due to the impedance mismatch observed in the small-signal characterization (Fig. 6.9).

The measured and simulated radiated power, power efficiency, and power gain of the active waveguide simulator at the P1dB level versus the frequency are plotted in Fig. 6.12. The measured large-signal performance of the AIUC prototype deviates from the simulations at frequencies below 28 GHz, caused by the impedance mismatch between the radiating element and the PA optimal load (see Fig. 6.9). Accordingly, P1dB radiated power reduction and thus decline in power efficiency are noticed at these frequencies. However, the power gain is higher than expected in this frequency range. Nonetheless, the AIUC prototype, demonstrating a peak 40% P1dB power efficiency, is considerably energy-efficient compared to the state-of-the-art AIAA designs (Table 6.1), in which the typical peak power efficiency at P1dB is around 20% or less.

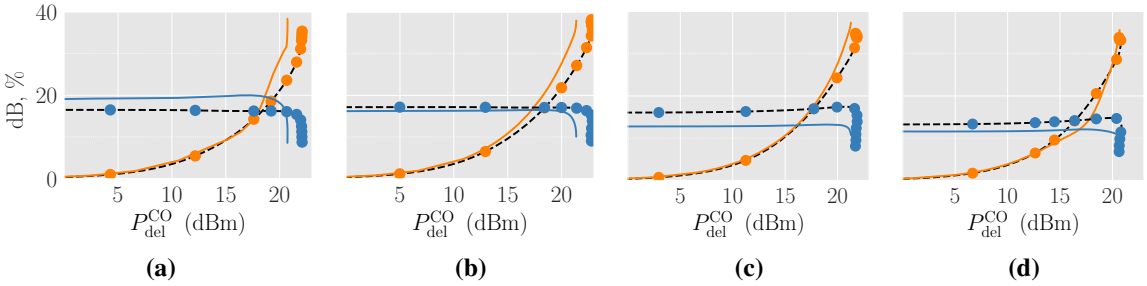


Figure 6.11: Simulated AIUC (dashed) and active WG simulator (symbols) as well as the WG simulator experimental results (solid) for power efficiency (η_a^{CO}) and power gain ($G_{\mathrm{P}}^{\mathrm{CO}}$) versus radiated power ($P_{\mathrm{del}}^{\mathrm{CO}}$) at (a) $f_0 = 27\,\mathrm{GHz}$, $\theta_s = 31.4°$; (b) $f_0 = 28\,\mathrm{GHz}$, $\theta_s = 30.2°$; (c) $f_0 = 29\,\mathrm{GHz}$, $\theta_s = 29.0°$; (d) $f_0 = 29.6\,\mathrm{GHz}$, $\theta_s = 28.4°$, beamsteering in the H-plane.

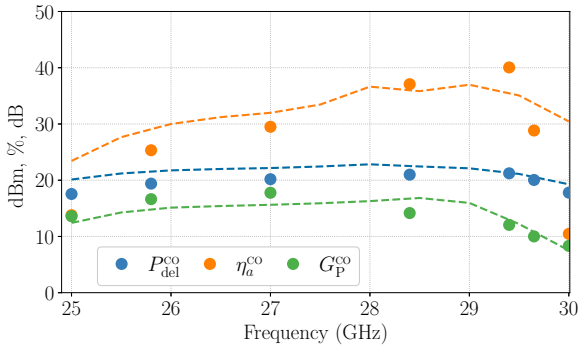


Figure 6.12: Measured AIUC radiated power, power efficiency, and power gain at 1 dB output power compression point plotted against the frequency. As observed in the small-signal result, the measured (symbols) large-signal performance deviates from the simulated (dashed) result due to impedance mismatch at the integration interface, leading to lower P1dB radiated power and thus lower power efficiency but higher gain at 25–27 GHz.

6.7 Manufacturing, Assembly, and Measurement Considerations

More challenges in manufacturing, assembly, and measurements occur in AIA designs than in passive antenna designs. For instance, the cavity-backed slot radiator's dimension is essential for realizing the desired antenna impedance, which, in turn, has a significant effect on the PA characteristics, e.g., PAE and saturated output power. Furthermore, the integrated E-plane probe's position relative to the slot radiator, especially in the E-plane, impacts the antenna impedance. Thus, it is critical to ensure that the manufacturer's tolerance capability meets the expectations and take approaches to reduce assembly misalignment.

Attention also needs to be paid to the measurement setup and associated measurement uncertainties. For example, the probe used in on-wafer characterization can impact the circuit stability and lead to PA oscillation at low frequencies ($<10\,\mathrm{GHz}$). When placing the AIUCs inside the active infinite array WG simulator, the higher-order harmonics (e.g., second and third harmonics) might experience severe multiple reflections in the WG due to poor impedance matching of

the WG-to-coaxial adapter at those frequencies. In worst case, it can lead to AIUC oscillations. Furthermore, due to employing a WR-28-to-2.92 mm adapter (operating from 26.5–40 GHz) in the small-signal and large-signal characterization of the WG simulator, the radiating conditions of the second and third harmonic cannot be defined through the measurement setup used herein. In Section 6.4, the simulated second- and third-order HDs are below -20 dBc (Fig. 6.8b). Based on the results, one can assume the second and third harmonic radiations are too little (relative to the fundamental signal) to have noticeable effects on the system performance.

6.8 Comparison with State-of-the-Art mmWave AIAAs

Table 6.1 summarizes the state-of-the-art AIAAs in the key performance metrics. It is noticeable that most integrated designs suffer from low power efficiency (typically $<$22% at P1dB), narrowband characteristics ($<$3% impedance bandwidth), low active gain ($<$14 dBi per element), and limited beamsteering capability (1D scan, $\leq \pm 30°$). The proposed AIUC design has demonstrated 40% power efficiency, 22 dBi active antenna again, 28 dBm EIRP per element at P1dB, with 11.3% efficiency bandwidth and $\pm 55°$ and $\pm 40°$ wide-angle scan range in the E-plane and the H-plane, respectively.

6.9 Conclusion

The AIUC is manufactured and characterized in the active infinite array waveguide simulator to verify the AIUCs operating in an infinite array scenario experimentally. The AIUC design example demonstrates a high performance large-scale active array, with 40% peak efficiency, 22 dBi peak active antenna gain, and 28 dBm peak EIRP per element at the 1 dB compression point. The AIUC features 11.3% fractional bandwidth (power efficiency $\geq$20%), with a scan range of $\pm 55°$ and $\pm 40°$ in the E-plane and the H-plane, respectively. Those experimental results have delivered the key parameters in the system design constraints (Table 3.1), enabled by applying the co-optimization methodology in AIUC designs and the efficient and broadband contactless transition with the on-chip E-plane probe.

Table 6.1: Performance comparison of state-of-the-art integrated active array antennas

	Center Freq. f_0, [GHz]	**Fractional Bandwidth [%] (Criteria)**	**Integration Technology**	**Configuration**	**Element Size**, $[\lambda^2]$	**Peak P1dB EIRP /El.** [dBm]	**Peak P1dB PAE**	**Peak P1dB Active Gain/El.** [dBi]	**Scan Range, Criteria**
[109]	5	2.2% ($S_{11} \leq -10$ dB)	Class A HJ-FET PA, PCB patch antenna (embedding IMN/OMN‡)	1×2 array	0.83×0.66	-1	19%†	11.5	AZ: 26° to 30° (N/A)
[110]	10	2% ($S_{11} \leq -10$ dB)	PCB patch antenna, FET PA-coupler-antenna	1×5 array	0.8×1.35	N/A	N/A	15.9 (5 El.)	N/A
[112]	26	N/A	Packaged class AB/C 0.15 µm GaN HEMT Doherty PA on SiC, backside transition to patch antennas	2×2 array	0.43×0.43 (array)	N/A	21.7%	13.5*	N/A
[113]	30	10.8% (VSWR$\leq$ 2)	TX module, LTCC, patch antenna with superstrates, bond wire	52 elements (2×2 subarray)	0.36×0.37	N/A	N/A	21 (52 El.)	AZ: ±30° (3 dB scan loss)
This work [**E**]	20	1.6% ($\Gamma_{in} \leq$10 dB)	GaN HEMT PA, PCB, bond wire, metallic antenna	AIUC (infinite array)	0.62×0.51	35	28%	13.2	E-PLN ±60° H-PLN ±37° (2.1 dB scan loss, $\eta_a \geq 25\%$§)
This work [**F**]	28	11.3% ($\eta_a \geq 20\%$)	GaAs *p*HEMT class AB PA, PCB signal/DC feed, metallic antenna, contactless transition	AIUC (infinite array)	0.56×0.54	28	40%	22	E-PLN ±55° H-PLN ±40° ($\eta_a \geq 20\%$)
This work [**F**]	28	14.1% ($\leq$ 6 dB EIRP loss)	GaAs *p*HEMT class AB PA, PCB signal/DC feed, metallic antenna, contactless transition	AIUC (infinite array)	0.56×0.54	28	40%	22	E-PLN ±50° H-PLN ±40° ($\leq$ 6 dB EIRP loss)

†simulated result *small-signal measurement ‡input/output impedance matching networks § operate in 2.5 dB gain compression

CHAPTER 7

CONCLUDING REMARKS AND FUTURE WORK

In the past decade, the mobile wireless communication evolution has shifted the operating frequency spectrum from the sub-6 GHz bands to the millimeter-wave (mmWave) frequencies to maximize the absolute bandwidth. However, this shift towards higher frequencies comes at the cost of increased free space path loss. This is an area where active integrated array antennas play an important role compared to conventional antenna systems realized with well-isolated and separately-designed system components (e.g., antenna, amplifier, filters) through a standard, typically 50 Ohm, interface impedance. Active integrated antennas allow for higher RF/mmWave output power to compensate for the increased path loss and reduce the antenna weight and form factor. However, the main challenge is integration for large-scale arrays of such active antenna elements due to a considerably smaller physical size and element spacing at higher frequencies. The power amplifiers, array signal routing, and interconnections must be confined within a half-wavelength element spacing with rectangular-lattice to enable wide-angle scanning arrays. At Ka/K bands, the half-wavelength spacing is between 3.7 mm to 8.3 mm, which places a stringent limit on the available physical space for accommodating all the active and passive electronics. The present-day antenna integration methods and technologies suffer from a relatively low energy efficiency due to the high power consumption and sizeable form factor, which are not applicable in energy-efficient wide-angle scanning arrays. This chapter summarizes the main conclusions of this Ph.D. work towards improved energy efficiency of active integrated array antennas at K/Ka bands and possible directions for future studies.

7.1 Concluding Remarks

I. Demonstrated a direct integration of the antenna radiating element and power amplifier at the K band without any intermediate and potentially lossy impedance matching network

and a harmonic tuning circuitry by synthesizing the PA optimal load impedance for maximum power-added efficiency (PAE), which is very different from 50 Ω, with the radiating element. The antenna radiating element is designed to match the optimal loading condition at the fundamental ($Z_{\text{opt}} = 17 + j46\ \Omega$), second and third harmonics for the maximum PAE and increased linearity of the PA-antenna integrated module, where the inter-element spacing is smaller than[1] $0.6\,\lambda$.

II. A metallic cavity-backed bowtie slot antenna type has been selected to allow for high directivity of the radiating element (the back edge of the cavity acts as a ground plane) and to satisfy the size confinement of $0.5\,\lambda \times 0.5\,\lambda$. The bowtie slot radiating structure allows for sufficient degrees of freedom in synthesizing the desired antenna resistance and reactance for direct integration with the PA output by varying the slot length and flare angle. The flared slot also produces wider impedance bandwidth, in terms of the PA optimal load impedance, than the traditional rectangular slot. An array of such antenna elements becomes an array of connected slots, leading to wideband and wide scan angle array performance.

   In this work, the metallic cavity-backed bowtie slot antenna infinite array has demonstrated a PA optimal impedance matching over a wide bandwidth (16.4%, 25.3–29.8 GHz) and with high radiation efficiency[2] (>93%) and wide scan ranges (±55°/±40°) in the principal planes in the infinite array scenario.

III. The on-chip contactless transition at the interface between the antenna and power amplifier, i.e., at the output DC block, has been proposed and designed in the GaAs technology as an E-plane open-loop probe. It provides active antenna feeding to the bowtie slot radiator without any additional interfacing component. The simulated results show a significant enhancement of the impedance bandwidth (16.4%) compared to less than 2% bandwidth of the initial antenna element; in the initial design, the rectangular slot and the PA were interconnected with a bond wire.

IV. The proposed co-design flow accounts for the electromagnetic coupling effects and nonlinear behavior of integrated active array antennas, which facilitates the design with an optimal impedance at the PA and antenna interface to maximize the saturated power, power efficiency, bandwidth, and linearity strategically.

V. The proposed co-design methodology has been applied in designing a wideband, wide scan angle active array antenna in the Ka-band, consisting of a two-stage class AB GaAs *p*HEMT MMIC PA with on-chip E-plane probe and a cavity-backed bowtie slot radiator. By utilizing the active integrated unit cell design approach and the active infinite array waveguide simulator technique, a Ka-band infinite array active integrated unit cell design has been experimentally verified, demonstrating a peak power efficiency of 40% and a

[1] λ represents the wavelength at the center frequency.
[2] Simulated results.

significantly enhanced bandwidth (11.3%, in terms of power efficiency $\geq$20%) with a scan range of $\pm$55°/$\pm$40° in the two principal planes, compared with the initial active integrated unit cell design ($<$1.5%).

This demonstration is valid for the beam steering angle from[1] 28.3° to 33.1° as defined by the free-space wavelength and the cutoff wavelength of the waveguide simulator. The simulated and measured results show good agreements on the power efficiency at 27 GHz to 29.6 GHz range. At frequencies below 27 GHz, the measurements show that power efficiencies greater than 25% can be achieved despite being different from the simulations. The discrepancies are influenced by the mismatch between antenna impedance and the optimal load impedance caused by the model accuracy or manufacturing and assembly tolerances.

7.2 Future Work

One possible future work is to apply the co-design methodology to higher frequency bands such as the W and D bands. Other future research can extend the system integration to the other front-end electronics based on the concluding remarks above. For instance, one intuitive future study is to extend the co-design methodology to low noise amplifier (LNA) and antenna integration for optimized noise figures and improved receiver sensitivity. Furthermore, the active antennas can be integrated with the PA, LNA, and diplexer and become integrated transceiving array antennas, which can play an essential role in MU-MIMO scenarios. On the other hand, future studies could address the thermal management issue in large-scale PA-integrated active array antennas. The proposed co-design methodology can be adapted and consolidated with thermal analysis to optimize the thermal transfer in large-scale integrated transmitter arrays and mitigate the heat dissipation problems.

[1] Correspond to the measurement frequency from 29.7 GHz to 25.8 GHz.

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